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Power electronics design for a 50 PAX hybrid-electric regional aircraft

M. Meindl[1] and M. Maerz[2]
Friedrich-Alexander-Universität Erlangen-Nürnberg, Institute of Power Electronics, Nuermberg, 90429, Germany

F. Hilpert[3] and C. Bentheimer[4]
Fraunhofer Institute for Integrated Systems and Device Technology IISB, Aviation Electronics, Erlangen,91058, Germany

The transition to sustainable aviation plays a crucial role and can be managed by power electronics. The Clean Sky 2 project GENESIS addresses the environmental sustainability of hybrid-electric 50-passenger (PAX) aircraft systems in a life cycle perspective to support the development of a technology roadmap for the transition to sustainable and competitive electric aircraft systems. This article has emerged from the GENESIS research and describes different options for power electronics in a hybrid-electric aircraft. Possible solutions and estimates for the power electronics for 2030, 2040, and 2050 are proposed. This paper presents the required power electronics components for a regional aircraft with a possible range of 1500 km. The power distribution system of the whole aircraft, the HV DC voltage, and the power electronic converters are analyzed. These converters are presented, calculated, designed, and specified. Particular reference is made to the converters' power density and efficiency. The wide band gap materials silicon carbide (SiC) and gallium nitride (GaN) are discussed for the design of the converters [1–3].

I. Nomenclature

AC	=	*Analog current*
BFOM	=	*Baliga figure of merit*
BV	=	*Breakdown voltage*
CCM	=	*Continuous conduction mode*
DC	=	*Direct current*
ESR	=	*Equivalent series resistance*
eV	=	*Electron volt*
FC	=	*Fuel cell*
GaN	=	*Gallium nitride*
GT	=	*Gasturbine*
hPA	=	*Hectopascal*
HV	=	*High voltage*
IGBT	=	*Insulated-gate bipolar transistor*
J-FET	=	*Junction-FET*
MOSFET	=	*Metal oxide semiconductor field effect transistor*
PAX	=	*Passenger*

[1] Research Assistant and PhD Student, Institute of Power Electronics, markus.meindl@fau.de, AIAA Member.
[2] Director Institute of Power Electronics, Institute of Power Electronics, martin.maerz@fau.de.
[3] Group leader Aviation Electronics, Aviation Electronics, florian.hilpert@iisb.fraunhofe.de.
[4] Power Electronics Engineer, Aviation Electronics, christian.bentheimer@iisb.fraunhofe.de.

PLECS	=	*Piecewise linear electrical circuit simulation*
PEMFC	=	*Polymer electrolyte membrane fuel cell*
PSFB	=	*Phase-Shifted Full-Bridge*
PWM	=	*Pulse width modulation*
$R_{DS,on}$	=	*Designation for the switch-on-resistance or a minimum contact resistance of a field effect transistor*
R_G	=	*Gate resistor*
SiC	=	*Silicon carbide*
SOFC	=	*Solid oxide fuel cell*
TLAR	=	*Top-level aircraft requirements*
V	=	*Voltage*
V_{DS}	=	*Drain-Source voltage*
WBG	=	*Wide-Band gap*

II. Introduction

Hybrid electric propulsion architectures are among the emerging technological innovations that promise a greener and more fuel-efficient aviation of the future. A related fact is that it is also economically attractive for potential operators. An ATR-42 is used as a reference aircraft and redesigned as a hybrid-electric aircraft for 50 passengers. Emissions from transport have increased sharply worldwide over the last fifty years [2]. In order to usher in this energy revolution in the aviation sector, power electronics are becoming an increasingly important component. Due to the high efficiencies that power electronics can achieve, it has recently become appealing for the aviation industry to enable the transition to electric and sustainable aviation. Aviation has a very high energy demand, in which power electronics will play a central role as an onboard energy distributor. Power electronics act as a link between the individual energy-generating and energy-consuming components and serve to distribute energy in the aircraft. For the design of the components in a hybrid-electric 50 PAX regional aircraft, there will be different time horizons considered, which emerged from the Clean Sky 2 Project GENESIS [4]. First, this paper will discuss the constraints of operating the power electronics at high altitudes, the selection of semiconductors, and the power requirements for the particular scenario. Then, in the next chapter, the design process for the respective power electronic converters and the results for the respective time horizons 2030, 2040, and 2050 are explained and given in detail. A motor drive inverter, generator drive inverter, battery DC-DC converter, fuel cell DC-DC converter, DC-AC grid inverter, and isolating DC-DC converter for low voltage supply are examined in detail and classified in the different time horizons. Depending on the time horizon, the aircraft is operated with a gas turbine, battery or fuel cell, and battery technology. The power electronics for energy distribution in the aircraft are adapted and designed accordingly.

III. Influence parameter for power electronics design

This section describes the influence parameters for the design of power electronics components. Safety and functional issues are discussed for the integration of power electronics in hybrid-electric aircrafts. The following points describe the essential physical issues. The choice of the semiconductor material is also explained.

A. Choice of HV DC bus voltage

The internal HV DC bus voltage is an important parameter for all power electronics converters. It influences many different topics, which are briefly discussed below. Four different voltage levels (800 V, 1500 V, 2000 V, and 3000 V) have been chosen for the analysis. A high voltage direct current (HV DC) bus voltage of 800 V is popular for the newest battery electric vehicle generation [5, 6]. Many experiences and field data are already available for this voltage class. Many aircraft manufacturers discussed higher voltage levels above 1 kV in the project, but safety concerns and empirical values still need to be included. Another reason is that higher voltages could be better for the efficiency of power electronics and other components. The only advantage of a higher voltage is that less current is required for the same power demand. This advantage is only noticeable through lower cable weights. Due to the continuous development of cables and the fact that superconducting cables may be used in the future, it makes sense to keep the HV DC bus voltage at 800 V. If the HV DC link voltage is increased, the creepage and clearance distances will also increase. Consequently, the physical size of the power electronic converters can be negatively affected if the creepage and clearance distances become too large, as discussed in the next point.

B. Creepage and clearance distances

An increase in the HV DC bus voltage increases the creepage and clearance distances. Consequently, the physical size of the power electronics converters can be negatively affected if the creepage and clearance distances become too high. A first rough assessment has been carried out according to the standard IEC EN60664-1 to give insight into the dependency from different HV DC bus voltage levels. The pollution degree 2 (usually only non-conductive pollution occurs, temporary conductivity caused by condensation is expected) has been used for the analysis. The dielectric strength of air decreases with the air pressure and, therefore, with the installation altitude.

This phenomenon describes Paschen's law. For installation altitudes above 2000 m above sea level, the clearance distances must be increased by an altitude correction factor [7]. The altitude correction factor according to the standard EN60664-1 is given in Table 1. For a typical flight altitude of 25000 feet (= 7600 meters), a correction factor of 2.13 has to be applied. The 50 PAX aircraft should have a typical altitude of 20000 feet (= 6090 meters), so a correction factor of 1.71 must be applied. The clearance distances depend on the impulse withstand voltages, which have been derived from the maximum breakdown voltages of the power semiconductors and the HV DC bus voltage. Table 2 shows the result of the insulation coordination analysis for the creepage and clearance distances.

Table 1 Altitude correction factor according to IEC EN60664

Altitude in m	Barometric pressure in hPa	Multiplication factor for clearance
2000	800	1.00
3000	700	1.14
4000	620	1.29
5000	540	1.48
6000	470	1.70
7000	410	1.95
8000	355	2.25

Table 2 Creepage and clearance distances for different HV DC bus voltages

V_{DC}	Creepage distance	Impulse withstand voltage	Clearance distance for < 2000 m altitude	Clearance distance for 6090 m altitude
800 V	4.0 mm	1200 V	0.2 mm	0.34 mm
1500 V	7.5 mm	2300 V	0.5 mm	0.86 mm
2000 V	10.0 mm	3080 V	1.0 mm	1.71 mm
3000 V	15.0 mm	4600 V	2.0 mm	3.42 mm

C. Derating due to cosmic radiation and switch-off voltage

It should be noted that power semiconductors at high altitudes are prone to cosmic radiation-induced failures because of the increased particle flux. High-energy particles can generate "single event burnout" failures. Measurements show that the applied DC link voltage should be limited to 50 % of the device's breakdown voltage for silicon devices (IGBTs = insulated-gate bipolar transistors) to preserve low failure rates. For silicon carbide devices (SiC MOSFETs = silicon carbide metal oxide semiconductor field effect transistors), a reduction of the breakdown voltage up to 65 % is recommended to obtain low failure rates [8].

Another important goal in power electronics applications is to minimize the stray inductance in power switching loops. A high parasitic inductance will lead to high over-voltage spikes during the switching events, requiring a higher breakdown voltage rating of the power semiconductors. The DC bus voltage is usually limited between 60 % and 70 % of the breakdown voltage. For example, for an 800 V DC bus, 1200 V rated power semiconductors, and for a 400 V DC bus, 650 V rated power semiconductors are recommended. The breakdown voltage of power semiconductors is the largest reverse voltage that can be safely applied without destroying the part, e.g., due to avalanche breakdown. The breakdown voltage of the power semiconductors cannot be chosen arbitrarily. There are some distinct voltage levels, which can be chosen from, e.g., 650 V, 750 V, 900 V, 1200 V, 1700 V, 3300 V, and 6500 V.

D. Choice of power semiconductors – SiC and GaN

The main components for all power electronic converters are the power semiconductors. They have a significant influence on the system design and the system properties. Silicon-based power semiconductors have been used in all power electronics applications for years. For low-voltage applications, silicon (Si) MOSFETs, and high voltage applications, silicon IGBTs were used. Roughly ten years ago, the first wide bandgap (WBG) power semiconductors based on silicon carbide (SiC) and gallium nitride (GaN) came onto the market [9]. WBG devices are a disruptive technology beginning to get market traction as it displaces silicon-based technologies in various key power electronics markets. The SiC power device revenue is expected to rise from $592M in 2020 to $2562M in 2025, with a compound annual growth rate of about 30% [10] with battery electric vehicles (BEV) as the main driver. The GaN power device revenue is expected to rise from $47M in 2020 to $1107M in 2025, with a compound annual growth rate of about 70%, with the consumer market as the main driver [11].

SiC and GaN are comprehensive bandgap materials with a comparably larger bandgap than other semiconductor materials. These WBG materials enable the realization of transistors with high blocking voltages and low on-resistance, especially compared to silicon-based semiconductors. Table 3 compares the properties of the semiconductor materials Si, SiC, and GaN (see Fig. 1). The higher the critical field of SiC and GaN underlines their usability at high voltages, the higher thermal conductivity of SiC facilitates thermal management. SiC and GaN power semiconductors enable the realization of power electronic systems with the highest power densities, efficiencies, and switching frequencies. This advantage is due to the significantly reduced switching and conduction losses of these wide bandgap semiconductors compared to state-of-the-art silicon-based IGBTs and MOSFETs.

Table 3 Comparison of material properties

Materials property	Si	SiC	GaN
Band gap (eV)	1.12	3.2	3.43
Critical field (10^6 V/cm)	0.3	3.0	3.3
Electron Mobility ($cm^2/(Vs)$)	1500	700	2000
Peak Electron velocity (10^7 cm/s)	1	2	2.5
Relative Dielectric Constant	11.9	10	9.5
Thermal conductivity (W/(cmK))	1.5	3.7	1.3
Baliga Figure of merit – BFOM (W/ cm^2)	1	392*	1416*

*Normalized to Si

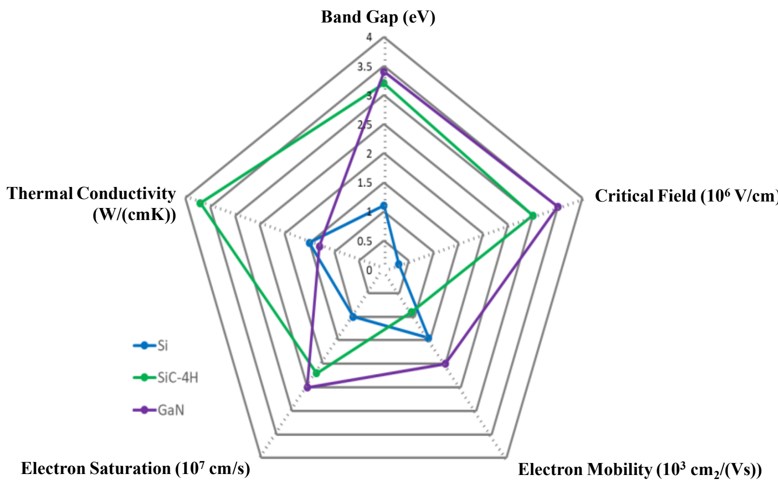

Fig. 1 Comparison of material properties [12]

<u>Slicon and silcon carbide</u>

For silicon-based semiconductors, an important choice is whether to use MOSFETs or IGBTs. IGBTs have a different internal build-up than MOSFETs. IGBTs have an additional PN junction that blocks reverse current flow, meaning that IGBTs cannot conduct current in a reverse direction like MOSFETs. An additional diode antiparallel to the IGBT is needed for an inverter application. Si MOSFETs, SiC MOSFETs, and GaN MOSFETs offer, in contrast to IGBTs, the possibility to conduct current in both directions with a so-called "body diode." This characteristic is used to carry the freewheeling current in inverter applications without additional external diodes. After the commutation process of the current is finalized, the transistors are turned on again, and their internal channel is used as a freewheeling path (synchronous rectification). Another drawback of IGBTs is that they are bipolar devices. The significant presence of minority carriers leads to long-tail currents during turn-off events and, therefore, too high turn-off losses. Additionally, the on-state forward voltage drop in IGBTs behaves very differently from power MOSFETs. The MOSFET voltage drop can be modeled as a resistance, with the voltage drop proportional to the current. By contrast, the IGBT has a diode-like voltage drop increasing only with the log of the current.

For the chosen 800 V DC bus voltage of the aircraft, it should be noted that only silicon IGBT can (typically) be considered for this voltage class. Silicon MOSFETs are only used for lower DC bus voltages. However, for comprehensive bandgap materials, the situation is different. Power semiconductors are only used in a MOSFET structure for these materials. Currently, no GaN IGBT is available, and some research work regarding SiC IGBTs is ongoing [13].

Overall, silicon carbide devices have many advantages regarding electrical properties compared to silicon devices. The only real drawback of SiC devices is that they are much more expensive nowadays. The price is expected to drop with growing demand, production ramp-up, and bigger wafer sizes. Even if there is no price equality at the device level, silicon carbide can bring advantages at system level. For example, the battery size can be reduced if power converters using silicon carbide power semiconductors have higher efficiencies. SiC devices also allow the usage of higher switching frequencies that reduce the size and weight of passive components (capacitors, inductors, transformers) and hence the size and weight of the power converters, which is very advantageous for aircraft applications. Altogether, for 2025-2035, SiC MOSFETs are the best option for all power converters. Some examples of commercially available SiC MOSFETs, considered for power electronics converters, are shown in Table 4.

Table 4 Some examples for market available SiC MOSFETs with low on-resistance values [14, 15]

SiC MOSFET	Package	V_{DS} in V	$R_{DS(on),25°C}$ in mΩ	$R_{DS(on),125°C}$ in mΩ	E_{on} in mJ	E_{off} in mJ	E_{ges} in mJ	I_{ref} in A	U_{ref} in V
SiC MOSFET A	Bare-Die	1200	9	13.3	3.50	0.70	4.20	100	800
SiC MOSFET B	Bare-Die	1200	16	24.8	2.82	0.15	2.97	80	800
SiC MOSFET C	Bare-Die	1200	16	21.6	2.12	0.62	2.74	75	800
SiC MOSFET D	Bare-Die	1200	16	22.4	6.25	1.10	7.35	100	800
SiC MOSFET E	Bare-Die	1700	20	34.0	0.77	0.23	1.00	75	1200

Gallium nitride

GaN is the newest class of market-available semiconductors with ongoing R&D work and technical improvement. All currently available GaN-transistors are lateral semiconductors as vertical GaN-technology is still in a research state with unknown readiness for market. The Baliga Figure of Merit (BFOM) is a unified performance metric for power semiconductor devices that considers the critical electric field and the mobility properties of the materials simultaneously. The BFOM value describes how well the component can operate at higher voltages and frequencies. The technology leap to vertical GaN would offer huge benefits like significantly reduced specific on-resistance, higher current densities, more even heat distribution, increased efficiency, and reduction in the size of passive components with higher switching frequencies. These advantages reduce overall the system size, weight, and costs. In order to take advantage of the full potential of GaN's material properties, homoepitaxially grown GaN substrates are an excellent approach for fabricating vertical power devices. The main disadvantage of epitaxial growth of GaN on Si or SiC wafers arises from a need for more agreement between the lattice constants of the materials. This effect causes high stresses in the epitaxial layer. These high stresses, in turn, lead to defects in the crystalline structure known as dislocations. These dislocations alter and degrade the electrical properties of GaN, cause low breakdown voltages, and are often the cause of poor device reliability. Therefore, it would be best to produce GaN-on-GaN, as shown in Table 5, to circumvent this physical barrier. However, GaN-on-GaN is still very expensive at this stage. For 2-inch GaN-on-GaN, the costs are currently 55-93 €/cm^2. In comparison, an 8-inch GaN-on-Si costs about 1 €/cm^2 [16, 17].

Table 5. Comparison of different types of GaN substrate [17]

Attribute	GaN-on-Si	GaN-on-SiC	GaN-on-GaN
Defect Density (cm^{-2})	10^9	$5x10^8$	10^3 to 10^5
Lattice Mismatch (%)	17	3.5	0
CTE Mismatch (%)	54	25	0
Layer Thickness (µm)	1-2	2-6	>40
Reliability	Low	Low	High
Device Types	Lateral	Lateral	Vertical & Lateral

Transistors have three terminals, namely gate, drain, and source. The source connection is the source of the electrons. At the gate terminal, the power flow (electron flow) between the source and drain is controlled by creating a potential barrier for electrons. The electrons then arrive at the drain terminal accordingly. The $R_{DS,on}$ (Designation for the switch-on resistance or a minimum contact resistance of a field effect transistor) is specified between the drain and source, determining the amount of current that can flow between the source and drain. A lower $R_{DS,on}$ means more current can flow (simplified: Ohm's law). With the new GaN-on-GaN scheme, a junction-FET (JFET) transistor can be built vertically, many times smaller than a lateral GaN-on-SiC transistor shown in Fig. 2. The GaN buffer layer can be bypassed with the vertical design, as explained above. For the same $R_{DS,on}$, the GaN-on-GaN transistor is four times smaller than a GaN-on-Si at a breakdown voltage (BV) of 600 V and seven times smaller at a BV of 1200 V. Since no GaN-on-Si HEMT is specified above a BV of 650 V, the estimation for 1200 V is purely fictitious. The limitations are as follows. As soon as the reverse voltage of the device exceeds the breakdown voltage, the electric field becomes too large and displaces free charge carriers from the lattice during collisions. These displaced charge carriers generate new charge carriers when colliding with lattice atoms. This snowball effect causes a sudden increase of free charge carriers, which causes an avalanche breakdown [16, 17].

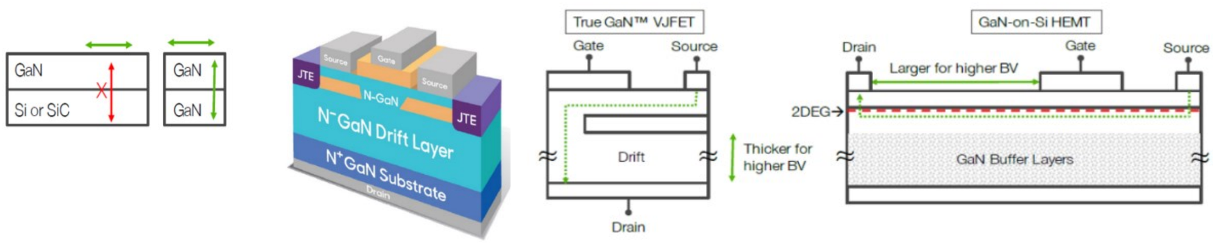

Fig. 2 GaN-on-GaN vertical, schematic of a true GaN VJFET transistor [17]

Overall, the competitiveness of GaN will strongly depend on its technological advancement within the following years. If it is possible to replace silicon devices with GaN devices soon, it would be possible to build more compact converters with a much higher density, as the electron mobility in GaN is ten times higher than in Si and 2.5 times higher than in SiC [17]. Fig. 3 shows a performance comparison of true GaN VJFET with respect to other devices. In this diagram, the BV is plotted over the $R_{DS,on}$. The ideal device would be in the lower right quadrant with a low $R_{DS,on}$, and a high BV. These measurements prove that GaN fulfills the best prerequisites for this and is highly justified for further research.

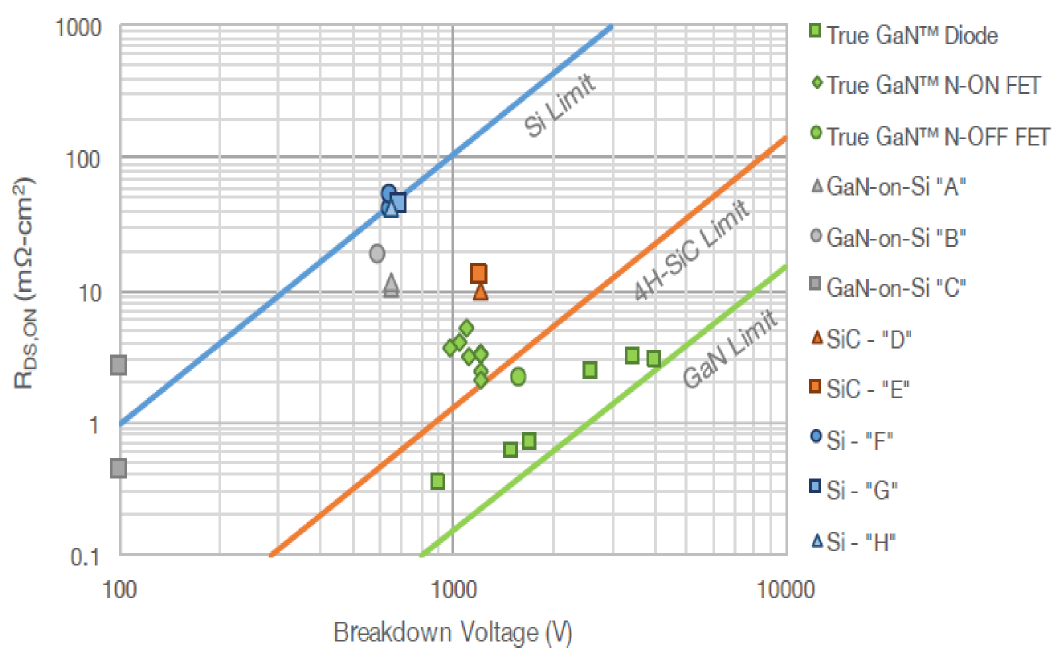

Fig. 3 Performance comparison of true GaN with respect to other devices [17]

Today, only a few GaN devices with reverse voltages of 900 V and 1200 V exist. They cannot compete with Si and SiC devices regarding on-resistance. For this reason, it was decided to use SiC devices for 2035-2045. In 2050, GaN devices will be an exciting alternative to SiC devices. SiC devices will be used for higher voltage, higher power, and medium frequency (<100 kHz) applications [11].

Overall, it can be concluded that silicon carbide and gallium nitride devices have many advantages regarding electrical properties compared to silicon devices (see Table 6). Given the insufficient breakdown voltage ratings and lack of components on the market, for years 2030 and 2040, SiC MOSFETs are the best option for all power converters. However, as already mentioned, GaN MOSFETs will be available in higher voltage classes in a few years. Therefore, integrating and testing a complete power electronic converter in this voltage range is difficult to estimate. Accordingly, the use of GaN MOSFETs is expected in 2050.

Table 6. Comparison of Si MOSFETs, Si IGBTs, SiC MOSFETs and GaN MOSFET properties

Parameter	Si MOSFET	Si IGBT	SiC MOSFET	GaN MOSFET
Device type	unipolar	bipolar	unipolar	unipolar
Breakdown voltage	12 V to 650 V	400 V to about 12 kV	600 V to several kV	12V to 650 V
Current density	medium	high	very high	very high
On-resistance $R_{DS(on)}$	medium	medium	low	low
Conduction losses	medium	medium	low	low
Switching speed	high	low	very high	very high
Switching losses	medium	high	low	low
Cost	low	medium	high	very high
Thermal conductivity	low	low	high	low

IV. Design requirements for a 50 PAX regional aircraft

In [2, 18–20], the basic top-level aircraft requirements (TLAR) for a hybrid electric 50-passenger regional class aircraft were defined. For 2025-2035, there will be two gas turbines and no fuel cell system. Two scenarios will be discussed for 2035-2045. One scenario considers gas turbines (GT/Hybrid) for the primary propulsion system and a battery system for the secondary propulsion system. The second scenario considers a fuel cell and a battery (FC/Hybrid) with only one propulsion system. For 2045-2055, a fuel cell system and a larger battery pack are envisaged. The two concepts are visualized in Fig. 4 for the introduction. The hybrid configuration with a gas turbine and the battery is shown on the left. On the right side of Fig. 4, the configuration of the fuel cell and the battery is shown. For the electric powertrain, a serial/parallel partial hybrid configuration was chosen [2, 20].

Furthermore, an overview and explanation of the performance requirements in a hybrid-electric aircraft, which the power electronics must fulfil, is given below. As in the aircraft design, a distinction is made between the two scenarios. For illustration purposes, Fig. 7 is the take-off phase shown for the GT-B scenario (2030). For a brief explanation, please refer to [2]. The power flow diagrams show that the electrical power from the battery system enters a bidirectional battery DC/DC converter, which transfers power from the battery with a maximum voltage of 681 V to the internal 800 V DC bus. The DC/AC grid converter and the isolating DC/DC converter supply the 400 Hz and 28 V power nets, respectively.

During take-off (see Fig. 7) power is transferred from the 800 V DC bus via the motor drive converters to the electric motors, which convert the electrical power into mechanical power to drive the secondary drive fans. The mechanical power from the gas turbine is transferred to a gearbox that drives the propeller of the main drive. In the start-up phase (Fig. 7), the gas turbine drives the electric generator via a second shaft in the gearbox. In this case, the inverter of the generator drive supplies additional electrical energy to the generator by rectifying the AC voltages to the internal 800 V DC bus. The energy required from the battery for the starting phase is 14 kWh. In the climb phase (Fig. 6), the energy demand of the battery increases to 273 kWh. With the additional electrical energy provided by converting the gas turbine power, the secondary electric motors assist in efficient and powerful take-off and climb flight. In the cruise flight phase (Fig. 7), the battery provides 558 kWh of energy and can thus significantly reduce emissions during the flight. Typically, the battery is expected only to be used as an energy source for take-off and climbing flights. However, in combination with a gas turbine, this propulsion strategy makes sense to reduce emissions through the hybrid-electric structure. The electrical energy from the battery system is also used via the battery DC/DC converter and the generator drive inverter to drive the main propeller in the cruise phase [2, 3, 20, 21].

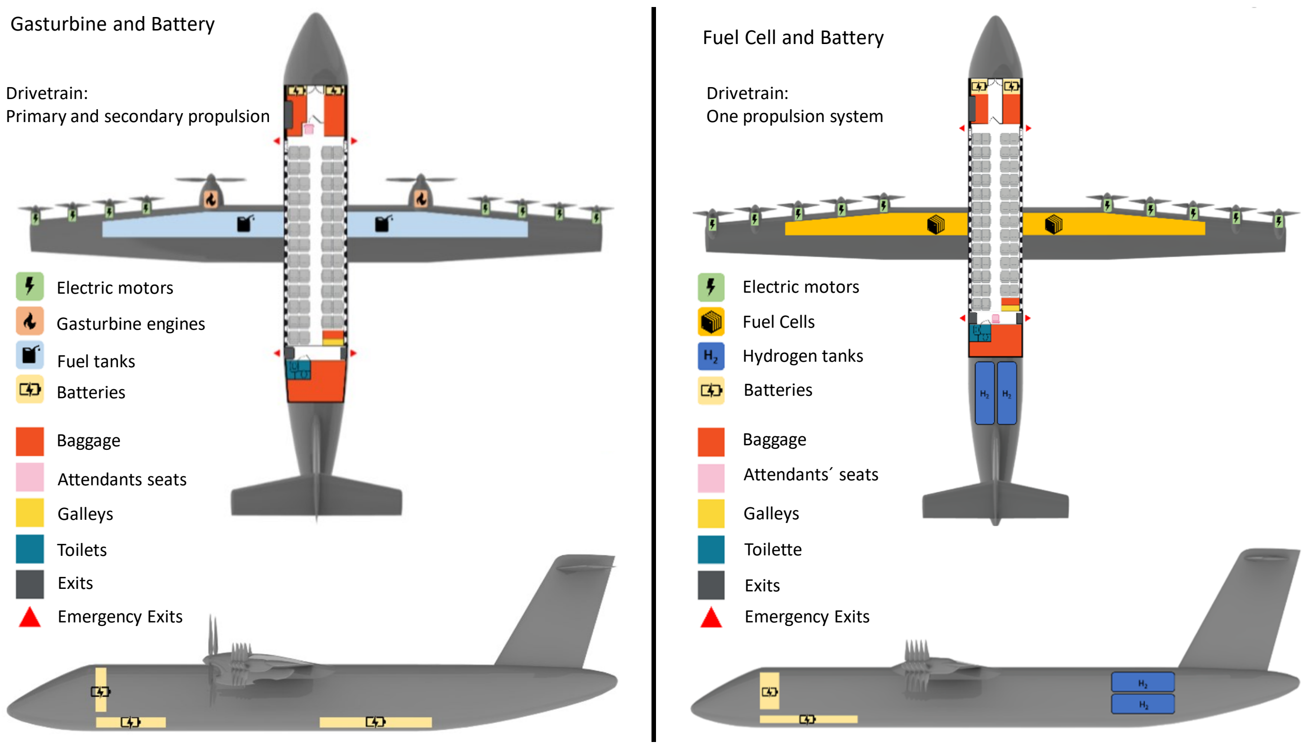

Fig. 4 Concept with gas turbine + battery (left) and concept of fuel cell + battery (right) [2]

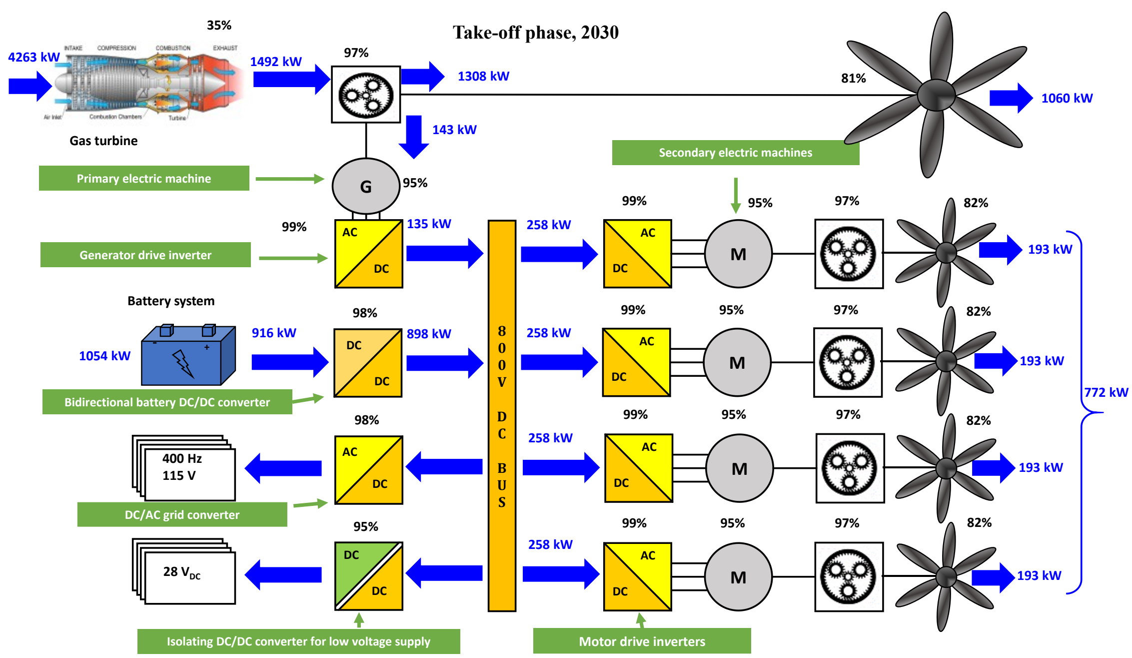

Fig. 5 Power flow take-off phase, 2030

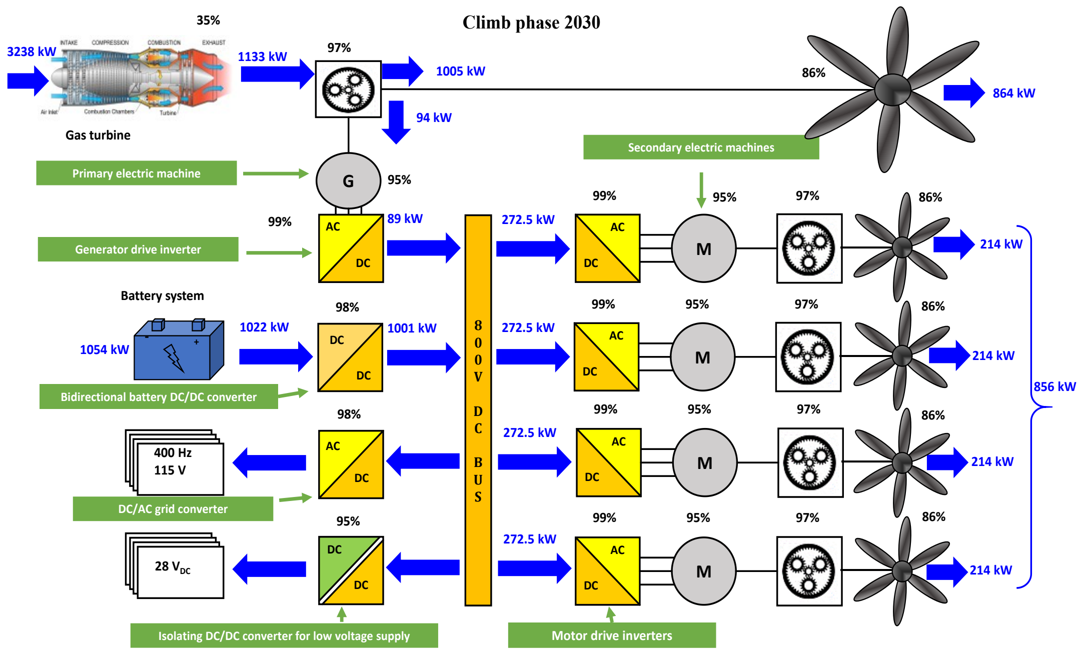

Fig. 6 Power flow climb phase, 2030

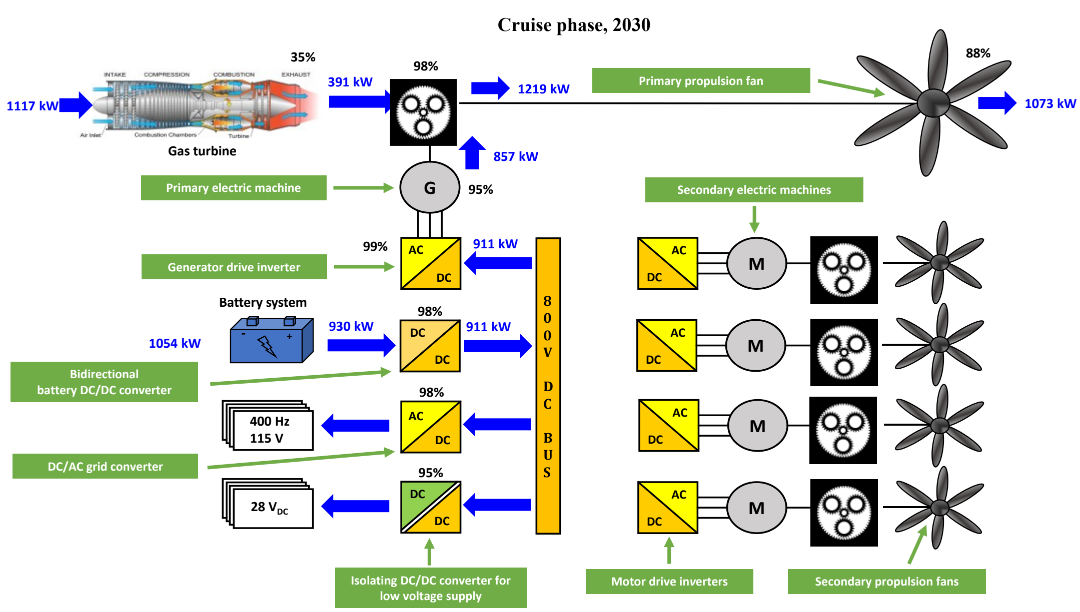

Fig. 7 Power flow cruise phase, 2030

A second scenario in the 2040 horizon includes the technological analysis of a hybrid aircraft consisting of a fuel cell and a battery. Fig. 10 shows the power distribution and power flow during the take-off phase. The power flow diagrams show that, as in the GT/hybrid scenario, the battery system provides electrical power, and the FC system replaces the GT power. During all three phases, power is transferred from the 800 V DC bus via the motor drive converters to the electric motors, which convert the electrical power into mechanical power to move all five propellers with the same power.

The chemical power of the FC is supplied to an FC DC/DC converter, which provides the DC bus. In the take-off phase (Fig. 10) the FC supplies most of the power demand to the internal 800 V DC bus. The power demand for liquid hydrogen in the take-off phase is 38 kWh, supported by 25 kWh of battery energy. In the climb phase (Fig. 9), the hydrogen energy demand is 782 kWh, and the battery energy demand is 440 kWh. Similar to the GT/Hybrid scenario, in the cruise phase (Fig. 10), the battery supports the fuel cells with 507 kWh, which have an energy demand of 820 kWh. The battery supplies the internal 800 V DC bus with the required power. The drive inverters' switching frequency is doubled from 20 kHz to 40 kHz in the FC-B scenario to increase the power density and reduce the weight of the electric motors. For this, higher inverter and motor losses must be accepted, reflected in a minimally worse efficiency of the inverters and motors. However, these are necessary due to the weight savings and the higher power density of the engines to achieve the ambitious weight targets and power densities. The design of the drive concept offers potential for changes. Still, the fuel cell and battery components can vary significantly in weight and size depending on the energy requirements; it is not part of this study and can be found in [2, 20, 21].

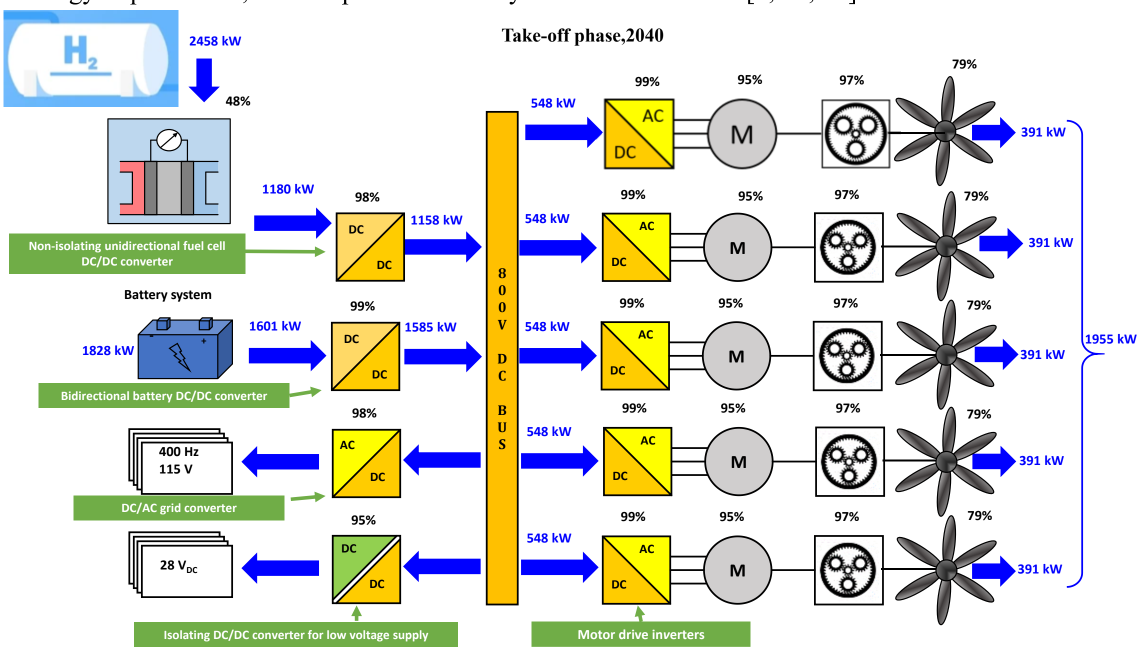

Fig. 8 Power flow during take-off phase, 2040

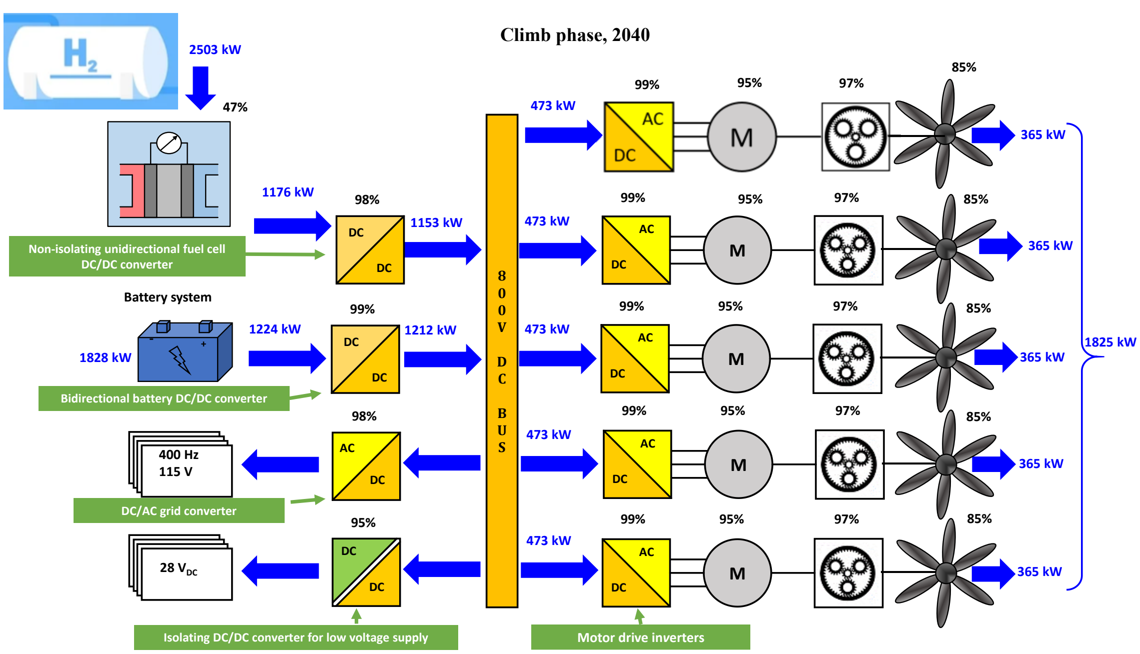

Fig. 9 Power flow during climb phase, 2040

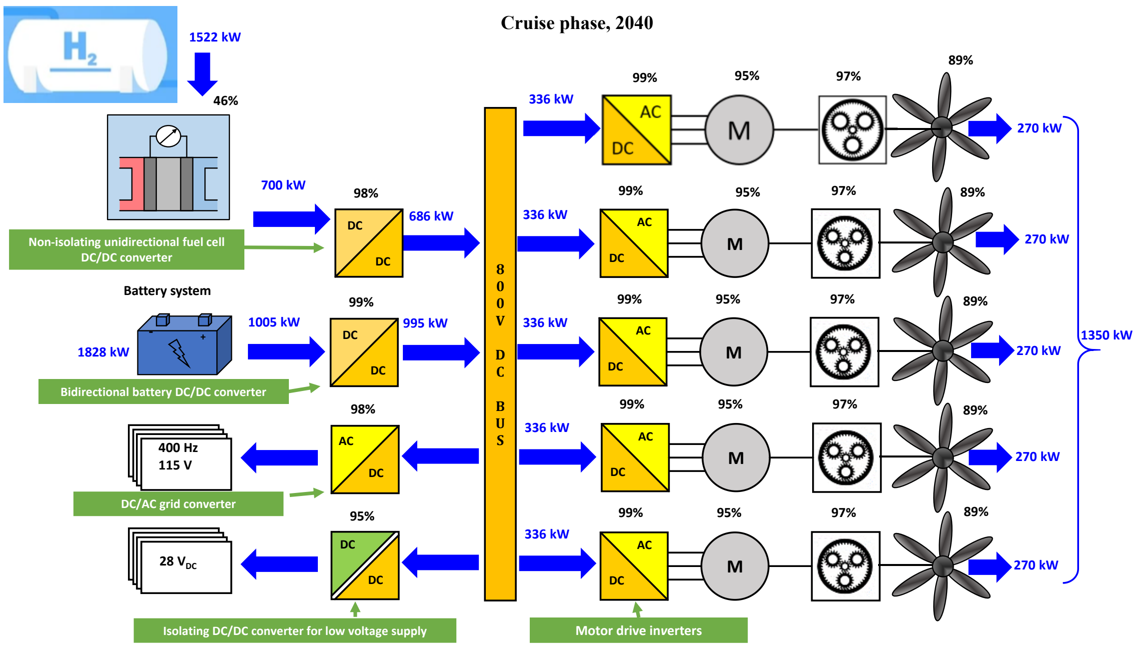

Fig. 10 Power flow during cruise phase, 2040

V. Development and results for power electronic converters

The following section outlines in general the design flow for the power electronics converters. The main equations and steps for the design are described in detail. The equations are based on physical laws and are accordingly valid for any time horizon.

E. Motor and generator traction drive inverter design flow

This section deals with the motor and generator traction drive inverters. For 2030, secondary machines will be a 290 kW six-phase machine, which a six-phase motor drive inverter will drive. The primary machine will be a further developed two-times stacked six-phase machine (554 kW), which two six-phase motor inverters will drive. For 2040 a fuel cell–battery (FC-B)/hybrid scenario with a 600 kW 6-phase inverter is planned. The inverter designs will be presented in Table 8 to Table 10

Table 9 shows the results for the simulated power losses and the calculated DC link parameters for the motor inverter for 2040. The motor drive inverter has a nominal power of 600 kW. The same SiC power modules as in 2030 (CAB760M12HM3 from Wolfspeed [28]) were used because it is the best option today to simulate this inverter. The 6-phase motor inverter will consist of six half-bridge power modules, and the two-times 6-phase generator inverters will have twelve half-bridge power modules. For the inverter systems, efficiencies greater than 99 % can be achieved. In addition, a power density of 64 kW/kg for the motor drive inverter is assumed.

The following assumptions were made for the calculation and theoretical design of the drive inverters in 2050: The specific on-resistance Ron is reduced from 2 mΩ/cm2 to 1 mΩ/cm2. With double-sided cooling in 2050, the thermal resistance is reduced from 0.4 K cm2/W to 0.25 K cm2/W, and the maximum permissible chip temperature is increased from 175°C to 225°C. The results for motor drive inverters are presented in Table 10. GaN will be used as power semiconductors in 2050. As well, two different fuel cells were under consideration. A further developed PEMFC and a solid oxide fuel cell (SOFC) with varying power requirements for the whole system. The switching frequency of the drive inverters in 2050 has been set to 40 kHz so that the electric motors' power density and weight requirements can be achieved. For this, higher inverter and motor losses have to be accepted, reflected in the minimally poorer efficiency of the inverters and motors. However, these are necessary due to the weight savings and the higher power density of the motors to achieve the ambitious weight targets and power densities. With the assumptions made and the calculations, a power density of 93 kW/kg can be completed in 2050.

In the following the theoretical calculations and procedures are described. One approach to determine the inverter efficiency is calculating the losses for different operating points with analytic equations 1-11. The equations are given in [7, 22, 23]. The losses in the DC link capacitor and the bus bars are neglected. The driving losses and the blocking losses are negligible for the given application. Dead time losses are also neglected here. Therefore, the total power losses of a transistor P_{tot} are the sum of the switching losses P_{sw} and conduction losses P_{cond}:

$$P_{tot} = P_{sw} + P_{cond} \tag{1}$$

If a linear dependence of the switching energies from the voltage and current levels is assumed, then the total switching losses for a two-level inverter are given by:

$$P_{sw} = 6 \cdot f_{sw} \cdot (E_{on} + E_{off} + E_{rr}) \cdot \frac{1}{\pi} \cdot \frac{\hat{\imath}}{I_{ref}} \cdot \frac{V_{DC}}{V_{ref}} \tag{2}$$

Where f_{sw} is the switching frequency, E_{on} is the turn-on switching energy, E_{off} is the turn-off switching energy, E_{rr} is the reverse-recovery energy, V_{DC} is the DC link voltage, V_{ref} is the reference voltage, and I_{ref} is the reference current. The linear dependence of the switching energies from the current and voltage levels is an approximation. The temperature dependence is also neglected for the numeric calculations, which is more important for IGBTs. The temperature dependence of the switching losses is small for SiC-MOSFETs and can be neglected for the first rough analytic design of the system. As stated in section III, the voltage drop across the transistors during the on-state differs for bipolar (IGBTs) and unipolar (MOSFETs) transistors. The voltage drop can be approximated according to Fig. 11.

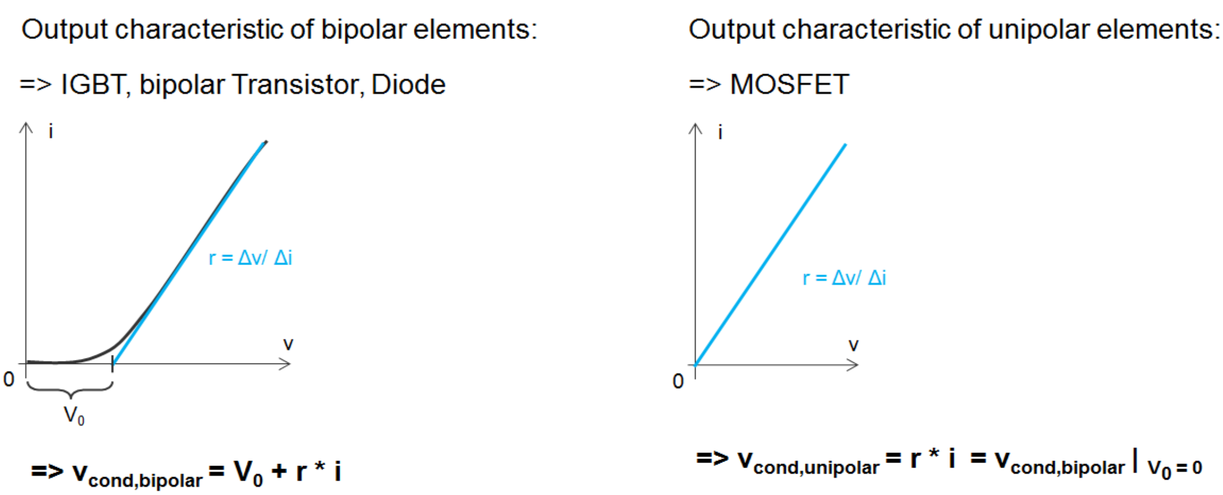

Fig. 11. Calculation of voltage drop for bipolar and unipolar semiconductors

For a unipolar transistor (MOSFET) with synchronous rectification, the conduction losses for the transistor $P_{cond,T,unipolar}$ and the internal body diode $P_{cond,D,unipolar}$ are:

$$P_{cond,T,unipolar} = R_{DS(on)} \cdot \hat{\imath}^2 \cdot \left(\frac{1}{8} + \frac{m \cdot \cos(\varphi)}{3\pi}\right) \tag{3}$$

$$P_{cond,D,unipolar} = R_F \cdot \hat{\imath}^2 \cdot \left(\frac{1}{8} - \frac{m \cdot \cos(\varphi)}{3\pi}\right) = R_{DS(on)} \cdot \hat{\imath}^2 \cdot \left(\frac{1}{8} - \frac{m \cdot \cos(\varphi)}{3\pi}\right) \tag{4}$$

Where $R_{DS(on)}$ is the on-resistance of the MOSFET, $\hat{\imath}$ is the peak output current, m is the modulation index, $\cos(\varphi)$ is the power factor, and R_F is the linearized on-resistance of the diode. Here, it is assumed that the on-state resistance for the MOSFETs is approximately the same for the first and third quadrant for the same gate-source voltage. The total conduction losses $P_{cond,unipolar}$ for a two-level inverter with unipolar transistors (MOSFETs) and synchronous rectification are:

$$P_{cond,unipolar} = 6 \cdot (P_{cond,T,unipolar} + P_{cond,D,unipolar}) = \frac{3}{2} \cdot R_{DS(on)} \cdot \hat{\imath}^2 \tag{5}$$

For high output currents, a parallel connection of two or more power devices is necessary. The total switching losses $P_{sw,T(n)}$ for a parallel connection of n transistors can be calculated as:

$$P_{sw,T(n)} = P_{sw,T} = f_{sw} \cdot (E_{on} + E_{off}) \cdot \frac{1}{\pi} \cdot \frac{\hat{\imath}}{I_{ref}} \cdot \frac{V_{DC}}{V_{ref}} \tag{6}$$

This means the total switching losses are independent of a parallel connection of several transistors. It is assumed that the current is equally shared between the devices, so each transistor generates $1/n$ switching losses. The same applies to the switching losses of the diodes $P_{sw,D(n)}$:

$$P_{sw,D(n)} = P_{sw,D} = f_{sw} \cdot E_{rr} \cdot \frac{1}{\pi} \cdot \frac{\hat{\imath}}{I_{ref}} \cdot \frac{V_{DC}}{V_{ref}} \tag{7}$$

The total switching losses $P_{sw}(n)$ for the two-level inverter with a parallel connection of n devices are:

$$P_{sw}(n) = P_{sw} = 6 \cdot \left(P_{sw,T} + P_{SW,D}\right) = 6 \cdot f_{sw} \cdot \left(E_{on} + E_{off} + E_{rr}\right) \cdot \frac{1}{\pi} \cdot \frac{\hat{\imath}}{I_{ref}} \cdot \frac{V_{DC}}{V_{ref}} \tag{8}$$

The transistor conduction losses $P_{cond,T,unipolar}(n)$ and diode conduction losses $P_{cond,D,unipolar}(n)$ for a parallel connection of n unipolar transistors with synchronous rectification can be calculated as:

$$P_{cond,T,unipolar}(n) = \frac{R_{DS(on)}}{n} \cdot \hat{\imath}^2 \cdot \left(\frac{1}{8} + \frac{m \cdot \cos(\varphi)}{3\pi}\right) \tag{9}$$

$$P_{cond,D,unipolar}(n) = \frac{R_F}{n} \cdot \hat{\imath}^2 \cdot \left(\frac{1}{8} - \frac{m \cdot \cos(\varphi)}{3\pi}\right) = \frac{R_{DS(on)}}{n} \cdot \hat{\imath}^2 \cdot \left(\frac{1}{8} - \frac{m \cdot \cos(\varphi)}{3\pi}\right) \tag{10}$$

The total conduction losses $P_{cond,unipolar}(n)$ for a parallel connection of n unipolar transistors with synchronous rectification for a two-level inverter are:

$$P_{cond,unipolar}(n) = 6 \cdot \left(P_{cond,T,unipolar}(n) + P_{cond,D,unipolar}(n)\right) = \frac{3}{2} \cdot \frac{R_{DS(on)}}{n} \cdot \hat{\imath}^2 \tag{11}$$

An iterative calculation would be necessary for a more accurate estimation of the power losses for each operating point. The on-resistance and the switching energies of power semiconductors are temperature-dependent, and so are the conduction and switching losses. The junction temperature will rise until a balance between the generated losses and the cooling is reached. Another possibility for estimating the inverter power losses is to use a simulation model, and the software tool PLECS® (= piecewise linear electrical circuit simulation) developed by Plexim can be used for such a task. Wolfspeed, the market leader in SiC production, has an online tool called "SpeedFit Design Simulator", which uses the software tool PLECS to estimate the losses of an inverter system based on input parameters such as operating point, switching frequency, and cooling conditions. The datasheet parameters of different SiC MOSFETs and power modules are already included in the simulation model. The results for the power losses of the motor and generator traction drive inverters obtained by the "SpeedFit Design Simulator" are shown in the next section (2030 and 2040). The losses have been calculated and simulated for a three-phase inverter used in a classic three-phase motor system belonging to the second electric machines. The primary electric machines are supplied by two identical inverters, also used for the secondary electric machines. The analysis showed that, for this system configuration, two power modules per phase would have to be connected in parallel to reduce the losses and not exceed the current capability of the power modules. To avoid the parallel connection of two power modules, it is possible to use a six-phase motor system with two separated star points (see Fig. 12).

For the three-phase solution, there would be one gate driver for two switches in two locally separated modules (see Fig. 13, left). The gate driver is placed in the middle of both switches as it cannot be simultaneously placed close to them. This placement results in a high parasitic inductance in the gate driver loop, which creates an oscillating circuit and leads to high ringing and voltage overshoots at the gate of the MOSFETs. Large gate resistors (Rg,on / Rg,off) are needed to dampen the oscillating circuit and prevent the destruction of the MOSFETs. Adversely, large gate resistors reduce the switching speed and lead to higher switching losses and lower efficiency.

For the six-phase solution, there would be one gate driver for one switch in one power module (see Fig. 13, right), allowing the gate driver to be placed very close to the corresponding switch. This placement results in a small parasitic inductance in the gate driver loop and an oscillating circuit, with much smaller ringing and voltage overshoots at the gate of the MOSFETs. Only small gate resistors (Rg,on / Rg,off) are needed to dampen the oscillating circuit. These enable higher switching speeds and lead to lower switching losses and higher efficiency, contrary to large gate resistors.

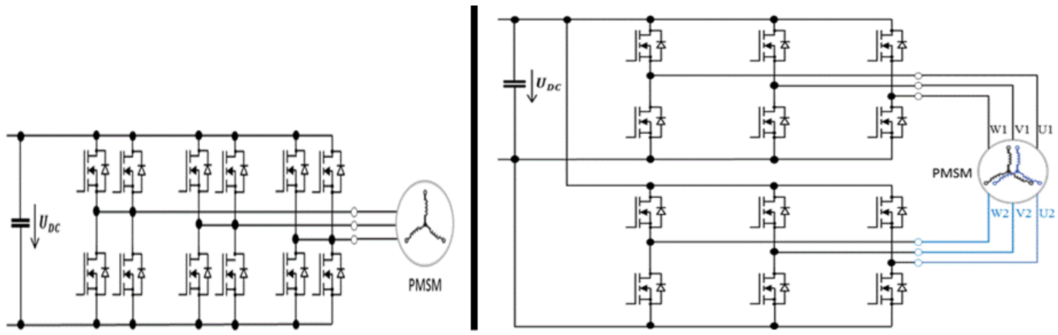

Fig. 12 Three-phase topology with paralleled devices (left) and six-phase topology (right)

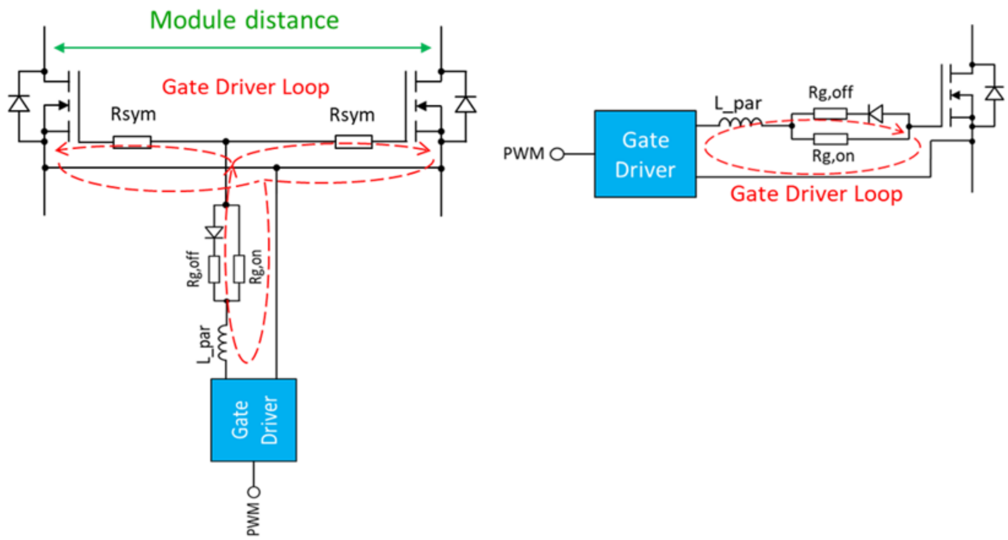

Fig. 13 Gate driver loop for three-phase configuration (left) and six-phase configuration (right)

To avoid the parallel connection of two power modules and increase efficiency, it was decided to use a six-phase configuration for the motor traction inverters for the secondary machines. This configuration results in a six-phase inverter system with one common DC link capacitor. For the six-phase system, the current and voltage ripple of the DC link and, therefore, the DC link capacitor can be reduced by using multiphase interleaved pulse-width modulated (PWM) techniques with phase displacement as stated in [24]. The total number of power semiconductors for the six-phase system remains the same as for the three-phase system. The total inverter losses of both systems are also approximately the same. Another advantage of the six-phase system is that this configuration enables fail-operational capabilities if incorporated into the control algorithm. If one of the two three-phase subsystems of the six-phase motor or the six-phase inverter fails, the other subsystem can still generate at least about half of the maximum output power and thrust for the aircraft. The disadvantage of the six-phase configuration is that a double number of current sensors and gate driver circuits are needed. However, it also has half the power requirements for each single gate driver output.

The DC link capacitor is the second most important part of the inverter system. A typical capacitor voltage ripple of less than 16 V is used for dimensioning the DC-link capacitor. The needed capacitance depends mainly on the maximum allowed voltage ripple, the switching frequency, and the operating point (voltage level, modulation index, phase angle) of the inverter system. For a six-phase system, the current and voltage ripple of the DC link and, therefore, the DC link capacitor can be drastically reduced. The first method uses multiphase interleaved PWM techniques and shifts the carrier signals for the PWM for the second three-phase system by a certain angle. The optimum angle value for the phase shift is 90 degrees. The second method is a motor phase displacement for the second three-phase system. The optimum angle value for the phase displacement is 60 degrees [24]. However, the difference between a phase displacement of 60 degrees and a value of 30 degrees is small, and for the current motor design, no phase displacement is planned. The required minimum DC link capacitance of a three-phase traction inverter can be estimated with equation 12 [25]:

$$C_{DC-link,min} \geq \frac{n \cdot I_{out}}{f_{sw}} \cdot \frac{1}{\Delta v_{pp}} \cdot R_{max}(\varphi) \tag{12}$$

With n the number of motor phases, I_{out} the output current amplitude, f_{sw} the switching frequency, Δv_{pp} the maximum allowed voltage ripple, and a scaling factor r_{max}, which depends on the output phase angle φ. The relevant values for the scaling factor R_{max} are shown in Table 7.

Table 7. Values for the scaling factor r_{max}

Angle	Value for 3-phase system	Value for 6-phase system
$\varphi = 20°$	$r_{max} = 0.061$	$r_{max} = 0.034$
$\varphi = 45°$	$r_{max} = 0.066$	$r_{max} = 0.025$
$\varphi = 70°$	$r_{max} = 0.071$	$r_{max} = 0.014$

The output phase angle φ lies, depending on the operation point of the motor, somewhat between 25° and 40°. For the dimensioning of the DC link capacitor, a factor of 0.034 for the six-phase system was used. The DC link capacitance can be calculated with the following equation:

$$C_{DC-link,min} \geq \frac{6 \cdot I_{out,6-phase}}{20\ kHz} \cdot \frac{1}{16\ V} \cdot 0.034 \tag{13}$$

The maximum ripple current is the second most important parameter for sizing the DC link capacitor. The ripple current generates losses inside the capacitors, which must be limited to not exceed the maximum allowed capacitor temperature. The ripple current depends on the motor's output current I_{out} and operating point (modulation index). For a 3-phase system, the maximum ripple current can be roughly estimated to be 60 % of the maximum output current I_0. For a 6-phase system, the maximum ripple current is reduced by a factor of 0.55 using interleaved PWM techniques [26]. Therefore, the maximum ripple current was calculated to:

$$I_{DC-link,max} = 0.6 \cdot 0.55 \cdot I_{out,6-phase} \tag{14}$$

For high-performance traction inverters, mainly foil or ceramic capacitors are used for the DC link capacitor. Electrolyte capacitors are too bulky to fit in the inverter design space and have a low current ripple rating. Ceramic capacitors have the highest capacitance volume density but are relatively expensive. Another drawback is that the capacitances of (most) standard ceramic capacitors are dependent on the applied voltage and temperature. They have very low equivalent series inductance and ESR (equivalent series resistance) values and a high ripple current capability, making them an ideal choice for DC link applications. The manufacturer TDK designed a unique series of ceramic capacitors called CeraLink™ [27], particularly suited for DC link applications. These capacitors are designed to have maximum capacitance at a voltage bias of 800 V and room temperature.

Foil capacitors have a rather low capacitance volume density but are relatively cheap compared to ceramic capacitors. The most significant advantage is that the capacitance of foil capacitors is neither voltage nor temperature-dependent. However, the maximum applied voltage is limited by the capacitor temperature. For example, for a temperature of 105°C, a derating of 70 % for the maximum allowed voltage is necessary. High temperatures also reduce the lifetime of foil capacitors dramatically. Due to higher ESR values, the ripple current capability is much smaller than for ceramic capacitors. The equivalent series inductance values are high because most foil capacitors are radial leaded devices. Ultimately, it was decided to use a custom-designed foil capacitor for the motor and generator drive inverters because it is more lightweight than a solution with ceramic capacitors. The capacitor solution would be smaller in volume, but the weight advantage should be favoured for an aircraft application. Using a custom foil capacitor makes it easier to use laminated busbars to connect the DC link capacitor with the power modules.

Results for motor drive inverter

This section deals with the forecast design requirements and results for the motor drive inverter for 2030, 2040 and 2050. Table 8 lists the calculated and simulated results for a primary and secondary SiC motor drive inverter according to the 2030 performance requirements. The power requirements can be found in section IV (Fig. 7) for the year 2030.

Table 8 shows the results for the simulated power losses with the "SpeedFit Design Simulator" and the calculated DC link parameters for the motor inverter for the primary machine. As explained, the generator inverter with a nominal power of 1108 kW consists of two motor drive inverters, each having a nominal power of 554 kW. Different SiC power modules were investigated, and the low-inductance half-bridge power module, CAB760M12HM3 from Wolfspeed [28], was chosen, because it is the best option today to simulate the inverter. The 6-phase motor inverter will consist of six half-bridge power modules, and the two-times 6-phase generator inverters will consist of twelve half-bridge power modules. For both inverter systems, efficiencies greater than 99 % can be achieved. In addition, a power density of 64 kW/kg for the primary converter is assumed. Table 8 also shows the results for the calculated DC link parameters. The motor inverter has a nominal power of 290 kW and the SiC half-bridge power module CAS480M12HM3 from Wolfspeed [29] was chosen. The 6-phase motor inverter can achieve a efficiency of around 99 % and a power density of 48 kW/kg [30].

Table 8 Results for motor drive inverter 2030 GT + Battery - SiC

	Definition		2030 Primary Take off	2030 Primary Climb	2030 Primary Cruise	2030 Secondary Take off	2030 Secondary Climb	Data Origin
Propeller		Mission time [min]	0.34 / 0.37	21 / 24	12 / 97	0.34 / 0.37	21 / 24	TLAR
	Mechanical power	$P_{Propeller}$ [kW]	1060	864	1073	193	212	TLAR
	Rotational speed	$n_{Propeller}$ [rpm]	1200	1200	1200	1200	1200	calculated
	Efficiency propeller	$\eta_{Propeller}$ [%]	81	86	88	82	86	TLAR
Electric motor	Efficiency gearbox	$\eta_{Gearbox}$ [%]	97	97	97	97	97	TLAR
	Gearbox ratio	Gearbox ratio	1:5	1:5	1:5	3:20	3:20	determined
	Mechanical power	$P_{Motor,mech}$ [kW]	141	313	949	243	254	calculated
	Torque	T_{Motor} [Nm]	238	530	1609	290	303	calculated
	Rotational speed	n_{Motor} [rpm]	5633	5633	5633	8000	8000	calculated
	Motor configuration	Phase number	2 x 6	2 x 6	2 x 6	6	6	determined
Inverter for electric motor	Inverter configuration	Phase number	2 x 6	2 x 6	2 x 6	6	6	determined
	Electrical power total	$P_{Inverter,total}$ [kW]	135	300	911	253	267	calculated
	Electrical power	$P_{Inverter,3\text{-}phase}$ [kW]	34	75	228	126	134	calculated
	Phase to phase current	$I_{LL,eff} = I_{str,eff}$ [A_{RMS}]	45	100	304	169	178	calculated
	DC voltage	V_{DC} [V]	800	800	800	800	800	determined
	DC current	I_{DC} [A_{RMS}]	171	378	1149	318	336	calculated
	Pulse-width modulation switching frequency	f_{PWM} [kHz]	20	20	20	20	20	determined
	Conduction losses	$P_{cond,total}$ [W]	107	321	2921	693	760	simulated
	Switching losses	$P_{sw,total}$ [W]	1294	2004	5352	1006	1052	simulated
	Inverter losses total	$P_{losses,total}$ [W]	1401	2325	8273	1668	1811	simulated
	Efficiency	$\eta_{Inverter,total}$ [%]	98.96	99.23	99.09	99.33	99.32	simulated
	Junction temperature	Tj [°C]	74	81	121	98	100	simulated
	DC link capacitor capacity	$C_{DC\text{-}link,min}$ [µF]	41	90	274	152	161	calculated
	DC link capacitor current	$I_{DC\text{-}link}$ [A_{RMS}]	30	44	201	111	118	calculated

Table 9 presents the prerequisites and results of the drive inverter for the motor in 2040 with Polymer Electrolyte Membrane Fuel Cell (PEMFC) and battery as energy source. SiC will be used as power semiconductors in 2040, because it is realistic that GaN isn´t ready in 2040 to implement in aircraft inverters.

Table 9 shows the results for the simulated power losses and the calculated DC link parameters for the motor inverter for 2040. The motor drive inverter has nominal power of 600 kW The same SiC power modules like in 2030 (CAB760M12HM3 from Wolfspeed [28]) were used, because it is the best option today to simulate this inverter. The 6-phase motor inverter will consist of six half-bridge power modules, and the two-times 6-phase generator inverters will consist of twelve half-bridge power modules. For the inverter systems, efficiencies greater than 99 % can be achieved. In addition, a power density of 64 kW/kg for the motor drive inverter is assumed.

For the calculation and theoretical design of the drive inverters in 2050, the following assumptions were made: The specific on-resistance Ron is reduced from 2 mΩ/cm^2 to 1 mΩ/cm^2. With double-sided cooling in 2050, the thermal resistance is reduced from 0.4 K cm^2/W to 0.25 K cm^2/W and the maximum permissible chip temperature is increased from 175°C to 225°C.

Table 9 Results for motor drive inverter 2040 PEMFC + Battery - SiC

	Definition		2040 Take off	2040 Climb	2040 Cruise	Data Origin
Propeller		Mission time [min]	0.34 / 0.37	21 / 24	12 / 97	TLAR
Propeller	Mechanical power	$P_{Propeller}$ [kW]	391	356	270	TLAR
Propeller	Rotational speed	$n_{Propeller}$ [rpm]	1200	1200	1200	calculated
Propeller	Efficiency propeller	$\eta_{Propeller}$ [%]	79	85	89	TLAR
Electric motor	Efficiency gearbox	$\eta_{Gearbox}$ [%]	97	97	97	TLAR
Electric motor	Gearbox ratio	Gearbox ratio	3:10	3:10	3:10	determined
Electric motor	Mechanical power	$P_{Motor,mech}$ [kW]	510	443	313	calculated
Electric motor	Torque	T_{Motor} [Nm]	1218	1057	747	calculated
Electric motor	Rotational speed	n_{Motor} [rpm]	4000	4000	400	calculated
Electric motor	Motor configuration	Phase number	6	6	6	determined
Inverter for electric motor	Inverter configuration	Phase number	6	6	6	determined
Inverter for electric motor	Electrical power	$P_{Inverter,total}$ [kW]	532	462	326	calculated
Inverter for electric motor	Electrical power	$P_{Inverter,3\text{-}phase}$ [kW]	266	231	163	calculated
Inverter for electric motor	Phase to phase current	$I_{LL,eff} = I_{str,eff}$ [A_{RMS}]	355	308	217	calculated
Inverter for electric motor	DC voltage	V_{DC} [V]	800	800	800	determined
Inverter for electric motor	DC current	I_{DC} [A_{RMS}]	671	582	411	calculated
Inverter for electric motor	Pulse-width modulation switching frequency	f_{PWM} [kHz]	40	40	40	determined
Inverter for electric motor	Conduction losses	$P_{cond,total}$ [W]	1299	956	475	simulated
Inverter for electric motor	Switching losses	$P_{sw,total}$ [W]	3818	3332	2396	simulated
Inverter for electric motor	Inverter losses total	$P_{losses,total}$ [W]	5117	4288	2871	simulated
Inverter for electric motor	Efficiency	$\eta_{Inverter,total}$ [%]	99.04	99.07	99.12	simulated
Inverter for electric motor	Junction temperature	Tj [°C]	115	107	93	simulated
Inverter for electric motor	DC link capacitor capacity	$C_{DC\text{-}link,min}$ [µF]	320	277	196	calculated
Inverter for electric motor	DC link capacitor current	$I_{DC\text{-}link}$ [A_{RMS}]	234	203	143	calculated

The results for motor drive inverters are presented in Table 10. GaN will be used as power semiconductors in 2050. As well two different fuel cells were under consideration. A further developed PEMFC and a solid oxide fuel cell (SOFC), with different power requirements for the whole system. The switching frequency of the drive inverters in 2050 has been set to 40 kHz so that the power density and weight requirements of the electric motors can be achieved. For this, higher inverter and motor losses have to be accepted, reflected in the minimally poorer efficiency of the inverters and motors. However, these are necessary due to the weight savings and the higher power density of the motors to achieve the ambitious weight targets and power densities. With the assumptions made and the calculations, a power density of 93 kW/kg can be achieved in 2050.

Table 10 Results for motor drive inverter 2050 - GaN

	Definition		2050 Take off PEMFC	2050 Take off SOFC	Data Origin
Propeller		Mission time [min]	0.34 / 0.37	0.34 / 0.37	TLAR
	Mechanical power	$P_{Propeller}$ [kW]	406	401	TLAR
	Rotational speed	$n_{Propeller}$ [rpm]	1200	1200	calculated
	Efficiency propeller	$\eta_{Propeller}$ [%]	77	77	TLAR
Electric motor	Efficiency gearbox	$\eta_{Gearbox}$ [%]	97	97	TLAR
	Gearbox ratio	Gearbox ratio	3:10	3:10	determined
	Mechanical power	$P_{Motor,mech}$ [kW]	544	537	calculated
	Torque	T_{Motor} [Nm]	1298	1282	calculated
	Rotational speed	n_{Motor} [rpm]	4000	4000	calculated
	Motor configuration	Phase number	6	6	determined
Inverter for electric motor	Inverter configuration	Phase number	6	6	determined
	Electrical power	$S_{Inverter,total}$ [kVA]	652	645	calculated
	Electrical power	$S_{Inverter,3\text{-}phase}$ [kVA]	326	322	calculated
	Phase to phase current	$I_{LL,eff} = I_{str,eff}$ [A_{RMS}]	370	365	calculated
	DC voltage	V_{DC} [V]	800	800	determined
	Inverter losses total	$P_{losses,total}$ [W]	1986	1961	calculated
	Pulse-width modulation switching frequency	f_{PWM} [kHz]	40	40	determined
	Chip area per switch	A_{chip} [mm^2]	52	51	calculated
	Chip area per subinverter	$A_{Inverter,3\text{-}phase}$ [mm^2]	310	306	calculated
	DCB area per subinverter	$A_{Inverter,3\text{-}phase}$ [cm^2]	31	30	calculated
	Efficiency	$\eta_{Inverter,total}$ [%]	99.45	99.45	calculated
	Base plate weight subinverter	M_{plate} [g]	81	80	calculated
	Volume DC link capacitor	$V_{DC\text{-}link,min}$ [cm^3]	77	79	calculated
	DC link capacitor weight (film capacitor)	$M_{DC\text{-}link}$ [kg]	0.08	0.079	calculated
	DC link capacitor weight (ceramic capacitor)	$M_{DC\text{-}link}$ [kg]	0.48	0.43	calculated

F. Bidirectional DC/DC converter

There are several suitable topologies for the bidirectional battery DC-DC converters. The main challenge is to choose the optimal solution for every individual application. The main requirements for the battery DC-DC converter in the scenarios are listed in Table 11.

Table 11 Summary main requirements Battery DC-DC converter

	2030	2040	2050 (PEMFC-B)	2050 (SOFC-B)
Output power	1055 kW	1828 kW	2233 kW	2265 kW
Battery voltage range	442 V / 664 V	476 V / 700 V	384 V / 723 V	381 V / 717 V
Battery nominal voltage	585 V	588 V	588 V	582 V
HV DC Bus voltage range	800 V	800 V	800 V	800 V
Galvanic isolation needed	No	No	No	No

In Table 11 is shown that the battery voltage ($U_{battery}$) is always lower than the HV DC bus voltage (U_{HV_DC}). From the battery to the HV DC bus, the converter will work as a boost-converter and from the HV DC bus to the battery as a buck-converter.

A simple half-bridge converter is also in 2040 an optimal topology. Fig. 14 (left) shows the proposed topology. It provides a simple, low-cost and highly efficient solution due to the low number of semiconductors and passive components. Furthermore, it is proposed to use three DC-DC converters in an interleaved configuration (see Fig. 10, right) to decrease the ripple current and, therefore, the losses in the inductors and capacitors. The size of the capacitors can also be reduced by using interleaved technology. Moreover, the number of parallel MOSFETs for a single converter without interleaving would be too high to construct a power module. The converter will be operated in continuous conduction mode (CCM) for better efficiency. As an example, the calculation of the converter for 2030 is described in equation 15 to 23. The value of the inductance in a half-bridge converter depends on both possible directions of energy flow. It is necessary to calculate the minimum inductor value for buck (L_{Buck}) and boost operation (L_{Boost}). The minimum value is determined according to the equations below:

$$L_{Buck} > \frac{V_{out} \cdot (V_{in\_max} - V_{out})}{K \cdot f \cdot V_{in\_max} \cdot I_{out}} \tag{15}$$

$$L_{Boost} > \frac{{V_{in\_min}}^2 \cdot (V_{out} - V_{in\_min})}{K \cdot f \cdot I_{out} \cdot {V_{out}}^2} \tag{16}$$

Where f is the PWM switching frequency, K is the estimated inductor ripple, V_{out} is the output voltage, I_{out} is the output current, V_{in_max} is the maximum input voltage. With an estimated 20 % inductor current ripple per converter, the inductance must be at least 28.37 µH. The voltage ripple ΔV_{max} is assumed to be less than 1 %. The capacitance and the ESR of the capacitor determine the voltage ripple. With the duty cycle D, the ESR-ripple for the buck-operation ($\Delta V_{out\_ESR\_Boost}$) and boost-operation ($\Delta V_{out\_ESR\_Buck}$) are given by:

$$\Delta V_{out\_ESR\_Boost} = ESR \cdot \left(\frac{I_{out}}{1-D} + \frac{\frac{K}{3} \cdot I_{out} \cdot V_{out}}{2 \cdot V_{in}} \right) \tag{17}$$

$$\Delta V_{out\_ESR\_Buck} = ESR \cdot \frac{K}{3} \cdot I_{out} \tag{18}$$

The minimum capacitance for the for the buck-operation (C_{out_Boost}) and boost-operation (C_{out_Buck}) is calculated to:

$$C_{Battery} = C_{out\_Boost} = \frac{I_{out} \cdot D}{f \cdot (\Delta V_{max} - \Delta V_{out\_ESR\_Boost})} \tag{19}$$

$$C_{HV\_DC} = C_{out\_Buck} = \frac{\frac{K}{3} \cdot I_{out}}{8 \cdot f \cdot (\Delta V_{max} - \Delta V_{out\_ESR\_Buck})} \tag{20}$$

For an assumed ESR of 1 mΩ, the capacitances are calculated to C_{out_Boost} = 280.2 µF and C_{out_Buck} = 14.09 µF. A maximum temperature increases of ΔT = 60 K was assumed for the MOSFET junction temperatures to calculate the necessary amount of parallel MOSFETs. The losses consist mainly of conduction losses and switching losses. The conduction losses P_{con} per MOSFET for the buck- or boost-operation can be calculated with the following two equations:

$$P_{con} = R_{DS(on)} \cdot \left(\frac{I_{out}}{n}\right)^2 \cdot D \tag{21}$$

$$P_{con} = R_{DS(on)} \cdot \left(\frac{I_{out}}{n}\right)^2 \cdot (1-D) \tag{22}$$

Where n is the number of parallel MOSFETs, $R_{DS(on)}$ is the on-resistance of the MOSFETs, and D the worst-case duty cycle of the buck or boost converter. Which one applies depends on the energy flow direction. The switching losses P_{sw} per MOSFET are estimated to:

$$P_{sw} = f \cdot (E_{on} + E_{off}) \cdot \frac{I_{out} \cdot V_{DC}}{I_{ref} \cdot n \cdot V_{ref}} \tag{23}$$

Where f is the PWM switching frequency, E_{on} is the turn-on energy, E_{off} is the turn-off energy, I_{out} is the output current, V_{DC} is the DC link voltage, I_{ref} is the reference current value, n is the number of parallel MOSFETs, and V_{ref} is the reference voltage value. The equation is simplified. There is no exact linear correlation between switching energies and current and voltage levels. The switching frequency is one of the main factors that determine the switching losses. There is a tradeoff between the size of passive components and switching losses. With a high switching frequency, the size of the capacitors and inductors can be reduced, but the switching losses will increase. A switching frequency of 100 kHz offers a reasonable tradeoff between size and losses.

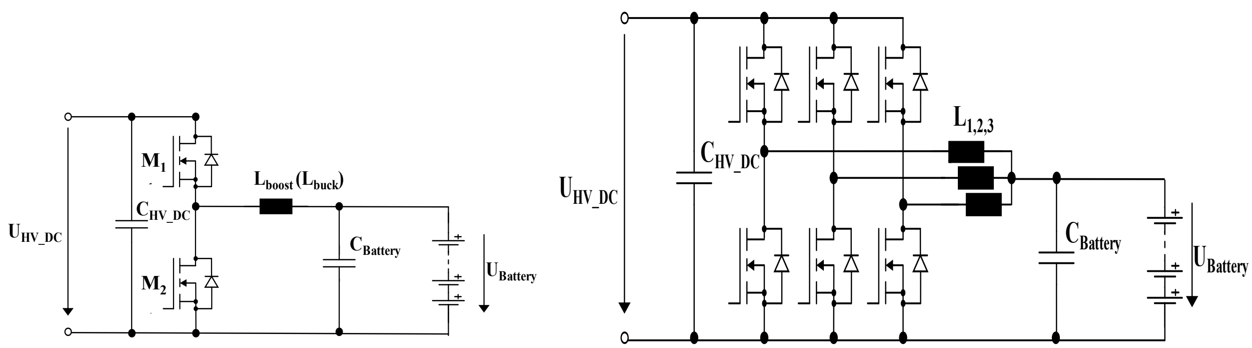

Fig. 14 Half-bridge DC-DC converter (left), three times interleaved half-bridge DC-DC converter (right)

The losses are multiplied by the thermal resistance to estimate the resulting temperature rise. Assuming low thermal resistance between MOSFET and heat sink, the minimum number of parallel MOSFETs is estimated in the scenarios of the different time horizons for M1 and M2 (see Fig. 14, left). The minimum number of parallel MOSFETs is given in the respective time horizons in the next chapters. Due to the specified maximum battery voltage of 723 V, power semiconductors with a minimum breakdown voltage of 1200 V must be used. Several options were considered, and finally, the 8.6 mΩ 1200 V SiC MOSFETs UF3SC120009K4S [31] from UnitedSiC were selected for the battery DC-DC converters.

Results for bidirectional battery DC-DC converter

For the design of the DC-DC battery converter, it was discussed with the battery experts in the project to design the converters with 10 kW more power in order to include a certain reserve margin. The design and calculation of the individual DC-DC converters was carried out according to the formulas shown above. The results are given in Table 12 for all time horizons. The calculations were carried out with SiC components.

Based on the research outlook assumed in section III, a rough estimate for a DC-DC converter can be given for 2045-2055 with GaN-MOSFETs. Compared to motor drive inverters, the higher switching frequency of 100 kHz positively influences the choke inductances, which can be reduced as a result. This influence leads to a more significant weight saving for the DC-DC converter. Therefore, using GaN components, the power density can be scaled up by a factor of 2 compared to the motor drive inverter.

To sum it up, it can be estimated that a factor of 2 can almost certainly be achieved in the time frame 2045-2055 and the power density could be about 100 to 130 kW/kg. These parameters and interpretations in this chapter were verified in expert discussions with Prof. Dr.-Ing Martin März [32] and Dr.rer.nat. Elke Meißner [33].

Table 12 Results for bidirectional battery DC-DC converter

Definition		2030	2040	2050-PEMFC	2050-SOFC	Data origin
M1 parallel		8	11	15	14	determined
M2 parallel		7	10	14	12	determined
Pulse-width modulation switching frequency	f_{PWM} [kHz]	100	100	100	100	determined
M1 losses	$P_{losses, M1}$ [W]	609	562	530	505	calculated
M2 losses	$P_{losses, M2}$ [W]	562	531	477	511	calculated
Temperature M1	$\Delta T, M1$	56-72	56-61	51-59	51-55	calculated
Temperature M2	$\Delta T, M2$	51-67	51-56	48-54	50-55	calculated
Efficiency buck	η_{Buck} [%]	99.53	99.6	99.6	99.6	calculated
Efficiency boost	η_{Boost} [%]	99.64	99.7	99.7	99.7	calculated
Power density	[kw/kg]	40-60	50-65	60-65	60-65	calculated /determined

G. Unidirectional fuel cell DC-DC converter

From 2035-2045, a fuel cell system is planned as the energy source. Therefore, a unidirectional fuel cell DC-DC converter is needed. However, the basic topology for such a converter would be a multi-interleaved boost converter, as shown in Fig. 14. Therefore, the same topology and design rules from Section F are used. The main requirements for the FC-DC-DC converter for the specific scenarios of the project are shown in Table 13.

Table 13 Summary main requirements Fuel Cell DC-DC converter

	2040 (PEMFC-B)	2050 (PEMFC-B)	2050 (SOFC-B)
Output power max.	1180 kW	1273 kW	1236 kW
FC system voltage	640 V	1280-1424 V	1068-1590 V
HV DC Bus voltage range	800 V	800 V	800 V
Galvanic isolation needed	No	No	No

Furthermore, it is proposed to use three DC-DC converters in an interleaved configuration (see Fig. 15). The converter will also be operated in continuous conduction mode for better efficiency. The value of the inductor in a half-bridge converter depends on the possible direction of energy flow, from the FC to the HV DC bus. But it is also necessary to calculate the minimum inductor value boost operation (L_{Boost}). The calculations are the same as in chapter F. For the FC-DC-DC converter the PWM switching frequency, the estimated inductor ripple, V_{out}, I_{out}, $V_{in,max}$ are also necessary parameters like for the battery DC-DC converter. Because of the similarity to the battery DC-DC, the switching frequency of the FC-DC-DC is also one of the main factors that determine the switching losses.

Assuming low thermal resistance between MOSFETs and heat sink, the minimum number of parallel MOSFETs is estimated in the scenarios of the different time horizons for M1 and M2 (see Fig. 15). The minimum number of parallel MOSFETs is given in the respective time horizons in the next chapters. Due to the specified maximum FC voltage of 640 V for 2040, power semiconductors with a minimum breakdown voltage of 1200 V must be used. Several options were considered, and finally, the 8.6 mΩ 1200 V SiC MOSFETs UF3SC120009K4S [31] from UnitedSiC were also used for the FC-DC-DC converters in 2040.

For the converters in 2050, a higher fuel cell voltage is expected than in 2040. Accordingly, the fuel cell converter will then be used in buck mode. The maximum fuel cell voltage will then be 1590 V. Accordingly, the 1200V SiC MOSFETS are no longer sufficient for the design. Therefore, the 410 mΩ 1700 V SiC MOSFETs UF3C170400K3S [34] from UnitedSiC were selected for the FC-DC-DC converters.

The theoretical calculated efficiency of the unidirectional FC-DC-DC converters is around 99.70 %. For the calculation, neither the inductor nor the capacitor losses were included. The actual reachable efficiency, in realistic application, should be about 98 % to 99 %. Using zero voltage switching to decrease switching losses might result in higher efficiency. This would require further investigation. Depending on the size of the inductors and capacitors, high sophisticated designs of the unidirectional FC-DC-DC converter should be enabled to reach a power density of about 60 to 70 kW/kg. Compared to motor drive inverters, there is a positive influence on the choke inductances, which are reduced. This results in greater savings on the DC/DC converter. Therefore, compared to the motor drive inverter, GaN components can be scaled by a factor of 2.

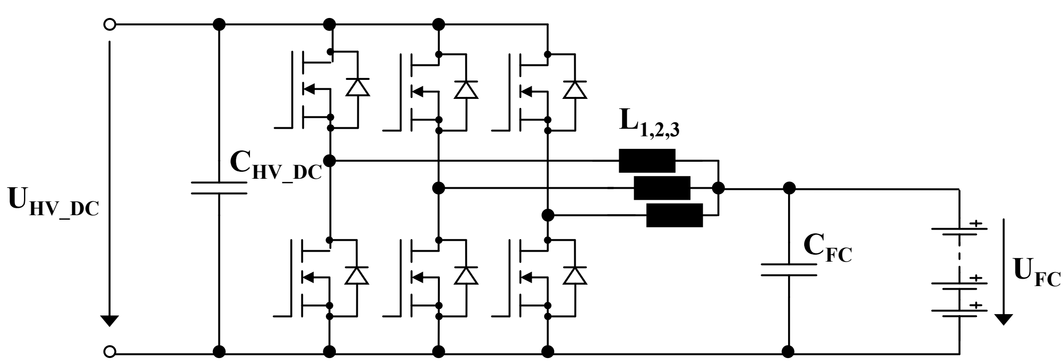

Fig. 15 Three times interleaved half-bridge DC-DC unidirectional FC converter

Based on the research outlook assumed in section III, a rough estimate for a 1237 kW DC/DC converter can be given for 2045-2055 with GaN-MOSFETS. It can be estimated that a factor of 2 can almost certainly be achieved in the time frame 2045-2055 and the power density could be about 120 to 140 kW/kg. These parameters and interpretations in this chapter were verified in expert discussions with Prof. Dr.-Ing Martin März [32] and Dr.rer.nat. Elke Meißner [33].

Table 14 Results of the FC-DC-DC converter for 2040 and 2050

Definition		2040	2050-PEMFC	2050-SOFC	Data origin
Semiconductor		8.6 mΩ 1200 V SiC MOSFETs	410 mΩ 1700 V SiC MOSFETs	410 mΩ 1700 V SiC MOSFETs	
M1 parallel		8	22	22	determined
M2 parallel		7	20	20	determined
Pulse-width modulation switching frequency	f_{PWM} [kHz]	100	100	100	determined
M1 losses	$P_{losses, M1}$ [W]	247	396	375	calculated
M2 losses	$P_{losses, M2}$ [W]	248	337	359	calculated
Temperature M1	$\Delta T, M1$	52	59	56	calculated
Temperature M2	$\Delta T, M2$	52	51	53	calculated
Efficiency	η [%]	99.7	99.7	99.7	calculated
Power density	[kw/kg]	60-70	60-70	60-70	calculated / determined

H. DC-AC grid inverter

The DC-AC grid converter has the basic topology of a two-level inverter, as described in section E (see Fig. 16). Therefore, the same design rules from section E apply to calculate the inverter losses and to size the DC link capacitor. The difference is that filter inductors must be connected between the DC-AC grid converter and the 400 Hz 115 V powernet to reduce the output current ripple. Depending on the requirements of the 400 Hz power net (harmonics current limits), it could also be necessary to increase the filtering effort and install a three-phase LC filter or LCL filter instead of only three inductors. The topic of electromagnetic compatibility and net filters is rather complex, needs extensive analysis, and is not part of this paper. However, a rough estimation of the filter inductance value is given here. The inductance value L_{filter} can be approximated to [7]:

$$L_{filter} \cong \frac{V_{DC} \cdot m}{2 \cdot \sqrt{3} \cdot f_{PWM} \cdot \Delta i_{max}} = \frac{800\,V \cdot 0.144}{2 \cdot \sqrt{3} \cdot 16\,kHz \cdot 5\,A} = 416\ \mu H \tag{24}$$

with V_{DC} the DC bus voltage, m the modulation index, f_{PWM} the PWM switching frequency and Δi_{max} the maximum allowed current ripple value. If required, a LCL-filter can, for example, be sized according to [35]. Table 15 shows the analysis results for the DC-AC grid inverter. The power semiconductor losses have been simulated with the "SpeedFit Design Simulator" from Wolfspeed. For the power semiconductors, the power module CAB425M12XM3 [36] was chosen. Sophisticated designs of DC-AC grid converters can reach a power density of at least 30 kW/kg for 2025-2035 and also for 2035-2045. Based on the research outlook assumed in section III, a rough estimate for a 30 kW DC-AC converter can be given for 2045-2055 with GaN-MOSFETS. It can be estimated that a factor of 1.7 can almost certainly be achieved in the time frame 2045-2035 and the power density could be about 51 kW/kg.

Table 15 Results of DC/AC grid inverter

Parameter	Value	Data Origin
Inverter configuration	3-phase	determined
$P_{Inverter,total}$ in kW	30	from TLAR
I_{DC} in A_{RMS}	38	calculated
V_{DC} in V	800	determined
$V_{out,LL}$ in V_{RMS}	115	from TLAR
f_{out} in Hz	400	from TLAR
f_{PWM} in kHz	16	determined
$P_{cond,total}$ in W	245	simulated
$P_{sw,total}$ in W	241	simulated
$P_{losses,total}$ in W	485	simulated
$\eta_{Inverter,total}$ in %	98.40	simulated
Tj in °C	84.2	simulated
$C_{DC\text{-}link,min}$ in µF	60.0	calculated
$I_{DC\text{-}link}$ in A_{RMS}	90	calculated

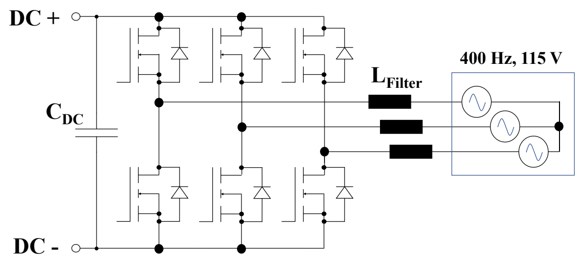

Fig. 16 DA-AC grid inverter

Based on the research outlook assumed in section III, a rough estimate for a 30 kW DC/AC converter can be given for 2045-2055 with GaN-MOSFETS. It can be estimated that a factor of 1.7 can almost certainly be achieved in the time frame 2045-2035 and the power density could be about 51 kW/kg.

I. Isolating DC-DC converter for low voltage supply

The isolating DC-DC converter for low voltage supply transfers power from the 800 V DC bus to the 28 V consumers of the aircraft. The total 28 V power demand per converter can differ for various regional aircraft. Table 16 shows two examples. The electric consumers inside the aircraft can explain the difference. The Bombardier CRJ100 has more electric consumers, which run on the 400 Hz power net, than the Embraer ERJ145. Therefore, the Bombardier CRJ100 has a higher power demand for the 28V power net than the 400 Hz power net. The Embraer ERJ145, by contrast, has a higher power demand for the 400 Hz power net than the 28 V power net. For this case study, a maximum output current of 400 A and a maximum output power of 11.2 kW for the isolating DC-DC converters were assumed. Five of these converters are also to be installed in the reference hybrid-electric aircraft design.

Table 16 Examples for 28 V power demand for two regional aircraft configurations

Regional aircraft	Number of units	Rated Voltage	Maximum Current	Maximum Power
Embraer ERJ145	5	28 V	400 A	11.2 kW
Bombardier CRJ100	5	28 V	100 A	2.8 kW

For the isolation between the high voltage and low voltage sides, a transformer is necessary. The transformer adds a significant amount of weight, decreases the system efficiency, and increases the system complexity. The isolating DC/DC converter for low voltage supply is the most challenging converter to design compared to the other presented power electronics converters. There are non-resonant, partial-resonant and resonant topologies. Fifteen different implementation possibilities of isolating DC-DC converters are described in [37]. For the given application, a LLC resonant converter or a phase-shifted full bridge (PSFB) converter are the two most promising candidates. The two topologies are shown in Fig. 17. They have the same number of power semiconductors, and both can use the same output stage (e.g., full bridge rectifier) on the low-voltage side. For higher efficiency, the diodes in the output stage are replaced by low-voltages silicon MOSFETs or, for very high switching frequencies, by low-voltage GaN-MOSFETs. The main difference between the two topologies is the control strategy. The output voltage of the LLC converter is controlled by changing the switching frequency, while the one of the PSFB converter is controlled by a phase shift of the PWM signals for the second half-bridge. Both topologies have distinct advantages and disadvantages. A short comparison of the properties is presented in Table 17 and more details can be found in [37] or [38].

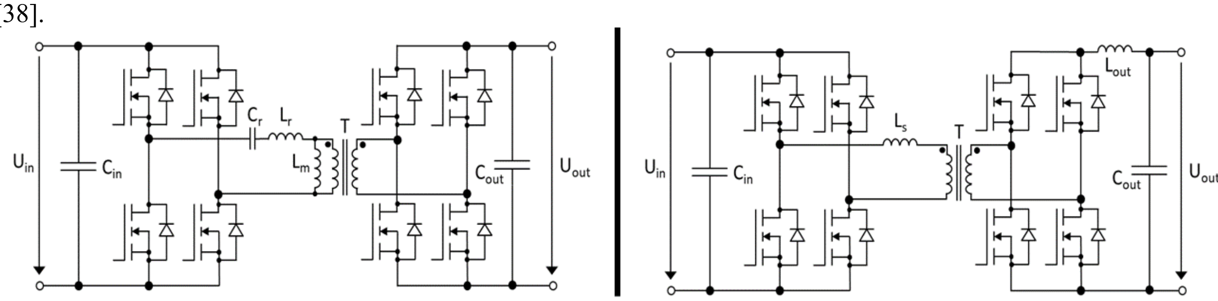

Fig. 17 LLC resonant converter (left), phase-shifted full-bridge (PSFB) converter

Table 17 Comparison between LLC and PSFB converter [38]

Parameter	LLC converter	PSFB converter
Switching frequency	variable	fixed
Synchronization, current share	poor	good
Output voltage range	medium	wide
EMI	low level of noise generation	medium level of noise generation
Efficiency	good, best at resonance	good, minimizes body diode conduction
Transformer	operates over a wider frequency range	fixed frequency range

An isolated 10 kW HV-LV-DC-DC converter is presented, which serves as a reference design for this converter class for 2025-2035 and also for 2035-2045. Fraunhofer IISB developed the converter for the LuFo V-3 project “GETpower 2”, which is (partially) funded by the German federal ministry BMWi. The main parameters of the converter are listed in Table 18. Regarding the power density, the developed reference design has a 2.5-times higher gravimetric power density than comparable state-of-the-art converters and a 2.3-timer higher volumetric power density. The basic structure of the converter is shown in Fig. 18. The converter is split into two identical building blocks. The HV input stage is connected in series to consider the breakdown voltage derating, which must be applied due to cosmic radiation and high altitudes. For the high voltage input stage, 1000 V SiC MOSFETs are used. The LV output stage is connected in parallel to increase the output current rating. The topology of the converter is a LLC resonant converter with a full-bridge rectifier output stage. In the output stage, 100 V silicon MOSFETs are used instead of diodes to increase efficiency. The mechanical design is shown in Figure 14. For 2040, this converter is more than sufficient. For 2040, it is expected that this converter would then be available for purchase and could be installed. For 2050 with an optimistic estimation, a power density of 5 kW/kg could be feasible for this DC/DC converter.

Table 18 Key parameters of the 11.2 kW isolating DC-DC converter

Parameter	Value	Unit
Input voltage range	540…840	V
Output voltage range	24…28	V
Maximum output current	400	A
Nominal output current	360	A
Maximum output power	11.2	kW
Nominal output power	10.0	kW
Volume	4	dm^3
Weight	5	kg
Volumetric power density	2.5	kW/dm^3
Gravimetric power density	2	kW/kg
Switching frequency	120…240	kHz
Efficiency	94…97	%

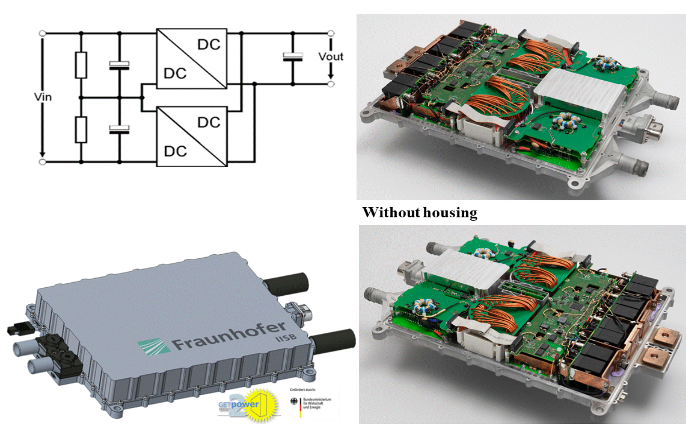

Fig. 18 Basis structure and mechanical design of the 11.2 kW isolating DC-DC converter

VI. Conclusion

This paper compares and estimates the power electronics components for a 50 PAX hybrid-electric regional aircraft for 2030, 2040, and 2050. Issues discussed include the constraints for operating the power electronics at high altitudes, the choice of power semiconductors, and the power requirements for each scenario. The focus is on different semiconductor types, and it is found that SiC is the best option for the 2030- and 2040-time horizons. GaN should be applicable in power electronic converters for hybrid-electric aircraft from 2050. The design processes for the respective power electronic converters and the results for the respective time horizons 2030, 2040, and 2050 are explained and presented in detail. Motor drive converters, generator drive converters, battery DC-DC converters, fuel cell DC-DC converters, DC-AC grid inverters, and isolating DC-DC converters for low-voltage supply were investigated in detail and classified in the different time horizons.

Different performance requirements for the power electronics in the different flight phases are presented, and the converters are designed and estimated according to the requirements. This study provides an initial assessment and classification of the requirements that power electronics can challenge and manage in an electric aircraft.

Acknowledgments

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