Aircraft drive inverter design at physical limits

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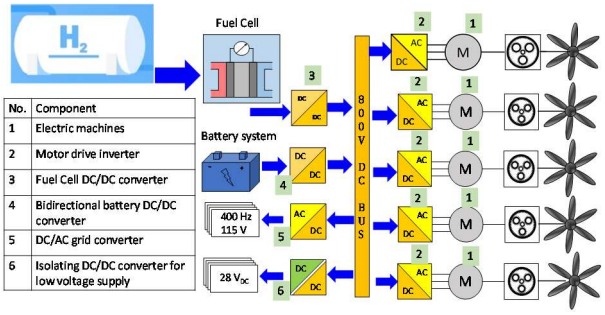
***Abstract* —Power electronics is a hotly debated and acutely researched topic for transitioning to sustainable aviation. Power electronic systems convince with high power densities and ensure the most efficient operation of the individual components in a hybrid-electric aircraft. This paper presents the first detailed considerations for exploring the drive inverter performance limits over different time horizons (2030 and 2050) in a hybrid-electric 50-PAX regional aircraft with a possible range of 1500 km. Based on many years of experience designing highly integrated drive inverters, the physical limits concerning power-to-weight ratio and efficiency were explored based on detailed analytical considerations, taking current component technologies and their extrapolated development potentials as a basis.**

Keywords—hybrid-electric aircraft, drive inverter, design limits

I. INTRODUCTION

The rising demand for air travel due to growing populations and prosperity has led to an increase of CO_2 emissions by 34 % within a timeframe from 2015 and 2020. The European Commission's "Green Deal" puts the aviation sector under great pressure by requiring Net Zero CO_2 emissions across all sectors by 2050. In 2020, the share of anthropogenic CO_2 emissions was approximately 2 to 3 %. With a projected growth rate of 4 % per year., drastic measures must be taken towards electrifying aircraft within different time horizons starting from today [1]. Power electronics are crucial to more sustainable mobility on land, at sea and in the air. Fig. 1 depicts the main electric system of a hybrid-electric aircraft composed of a fuel cell, a battery pack, and five electric motors. As can be seen, several power electronics converters are necessary for power distribution in this potential propulsion architecture, which has been extensively studied and already published in the GENESIS project [2] and publications [3–7]. The drive converters for the optimal operation of electrical machines such as generators and motors are particularly interesting for the drive system. Efficiencies of 99 % and more are expected from these power electronic components.



No.	Component
1	Electric machines
2	Motor drive inverter
3	Fuel Cell DC/DC converter
4	Bidirectional battery DC/DC converter
5	DC/AC grid converter
6	Isolating DC/DC converter for low voltage supply

Fig. 1. Overview of possible power electronics converters

For this reason, the technology-related performance limits of drive inverters are considered and discussed in detail in this paper. The theoretical limits are derived from a mathematical model. Assumptions and expert estimates for critical components are incorporated into this model, enabling a cornerstone to serve as a reference for identifying trends and revealing areas where significant improvements may be required to fly with zero carbon emissions.

For the timeline until 2030, a one-sided chip cooling is considered here. For the longer time horizon, double-sided cooling is taken into account. Since wide band gap power semiconductors (WBG) can be regarded as almost ideal in their dynamic behaviour at the switching frequencies relevant in drive inverters, no differentiation was made between silicon carbide (SiC) MOSFETS and gallium nitride (GaN) HEMTs. The influence on the target parameter's power density and efficiency is comparatively small, so all the considerations are performed assuming SiC MOSFETs.

The DC link capacitor is the dominant component of a drive inverter in terms of volume and weight. Since this component is exposed to high current stress, there is great potential concerning the key performance indicators of an inverter through a suitable choice of capacitor technology and careful thermal design. The major challenge here is reconciling the requirements regarding electromagnetic

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compatibility, manufacturability, and reliability. The pros and cons of using film or ceramic (MLCC) capacitors in the DC link are discussed [3, 8, 9].

II. CRITERIA AND REQUIREMENTS FOR INVERTER DESIGN

This section of the paper briefly explains the chosen design assessment approach. Based on the state-of-the-art of 2023 drive inverter 2-level topologies, the technological development potential for an inverter's relevant components and technologies were extrapolated for a long-term horizon of 2050. In addition to advances in power semiconductors, this includes improvements in heat dissipation, thermal management and passive components.

Table I [10] lists the electric motor's mechanical power requirements for 2050. Based on these requirements and for comparison, the inverters are designed and evaluated for these parameters. Expert assumptions listed in Table II are the first rough requirements expected for inverters in 2030 and 2050.

TABLE I. REQUIREMENTS FROM AIRCRAFT MANUFACTURER - AIRCRAFT PROPULSION SPECIFICATION

Parameter	2030/2050
Propeller power requirements	406 kW
Gearbox efficiency	97 %
Propeller efficiency	77 %
Required mechanical power	544 kW

TABLE II. ASSUMPTIONS FOR INVERTER SYSTEMS IN 2030 AND 2050, INCLUDING COOLING

Parameter	2030	2050
Specific on-resistance per square ($R_{on}^{(A)}$)	$2\ m\Omega \cdot cm^2$	$1\ m\Omega \cdot cm^2$
Cooling	*Unilateral*	*Bilateral*
Thermal resistance per square ($R_{th}^{(A)}$)	$0.4\ \frac{K \cdot cm^2}{W}$	$0.25\ \frac{K \cdot cm^2}{W}$
Maximum chip temperature ($T_{j,max}$)	*175 °C*	*225 °C*
Maximum coolant temperature	*65 °C*	*65 °C*
Maximum temperature swing at chip ΔT	*110 K*	*160 K*

III. METHODOLOGY AND DESIGN CONDITIONS

In what follows, the heat sink design is conducted (a). After that, the required active chip area is calculated (b) and the capacitor volume is estimated (c).

a) Cooling

A plate-fin structure was assumed for the cooling calculation. The design is based on a sample geometry and a subsequent scaling to the base plate to determine an area-specific thermal resistance. The fin gaps are shown for the base plate in Fig.2. Where h_f is the fin height, $d_f$is the fin gap, $s_f$is the fin thickness, W_{cc} is the heat sink width, l_{CC} is the heat sink length, λ_{hs} is the specific thermal conductivity of the heat sink material, d_{ground} is the base plate thickness, Δp is the allowable pressure drop, v_c is the kinetic viscosity, ρ_c is the specific weight, λ_c is the thermal conductivity of the coolant and c_c is the specific heat capacity of the coolant. The power semiconductors, the filter inductor(s), capacitor(s), and control circuits are directly mounted above this plate-fin cooling structure to reach a high-power density. Additional advantages of this design approach are minimised circuit parasitic elements, effective active and passive components heat dissipation, and tuned component geometries to minimise dead volumes [11].

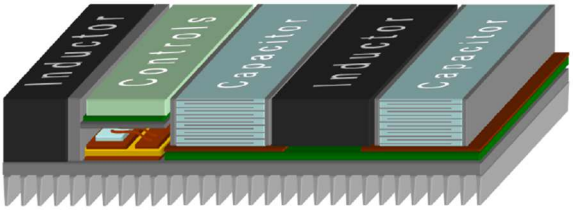

Fig. 2. Sophisticated thermal management and components that minimise dead volume and circuit parasites are the key to highly compact inverter designs [11].

To calculate the cooling performance, the hydraulic diameter of the fin gap (D_h; 1), average flow velocity in the fin gap (v_{cf}; 2), Reynolds number (Re; 3), Prandtl number (Pr; 4), Nusselt number (Nu; 5), the resistance of the heat sink (from the base plate to coolant outlet - R_{th}; 6), flow velocity at a given pressure drop (v_{cfp}; 7) and the volume flow at a given pressure drop (V_{flow}; 8) must be calculated at first [11].

$$D_h = 2\frac{h_f \cdot d_f}{h_f + d_f} \tag{1}$$

$$v_{cf} = \frac{V_{flow}}{h_f \cdot W_{cc}} \cdot \left(1 + \frac{s_f}{d_f}\right) \tag{2}$$

$$Re = \frac{v_{cf} \cdot D_h}{v_c} \tag{3}$$

$$Pr = \frac{v_c \cdot \rho_c \cdot c_c}{\lambda_c} \tag{4}$$

$$Nu = 0.023 \cdot Re^{0.8} \cdot Pr^{0.4} \tag{5}$$

$$R_{th} = \frac{d_{ground}}{\lambda_{hs} \cdot W_{cc} \cdot l_{CC}} + \frac{1}{c_c \cdot \rho_c \cdot V_{flow}} \cdot \left(1 + \frac{Re \cdot Pr}{Nu} \cdot \frac{h_f}{l_{CC}} \cdot \frac{1}{1 + 2\sqrt{\frac{s_f}{d_f}} \sqrt{\frac{\lambda_{hs}}{\lambda_c \cdot Nu}} \tanh\left[\sqrt{\frac{h_f}{d_f}} \sqrt{\frac{h_f}{s_f}} \sqrt{\frac{\lambda_c \cdot Nu}{\lambda_{hs}}} \right]} \right) \tag{6}$$

$$v_{cfp} = \left(\frac{2 \cdot \Delta p \cdot D_h^{\frac{5}{4}}}{0.316 \cdot \rho_c \cdot l_{CC} \cdot v_c^{\frac{1}{4}}} \right)^{\frac{4}{7}} \tag{7}$$

$$V_{flow} = \frac{W_{cc} \cdot h_f}{\left(1+\frac{s_f}{d_f}\right)} \cdot v_{cfp} \quad (8)$$

The specific thermal resistance $R_{th}^{(A)}$ (9) can be described from these equations as a function of fin spacing d_f, fin thicknesses s_f, and fin height h_f. This relationship, which yields this design's physical limits, is depicted in Fig.3 for pure water and a water-glycol mixture assuming aluminium as a heatsink material.

$$R_{th}^{(A)}(h_f, d_f, s_f) = R_{th}\left(h_f, d_f, s_f, V_{flow}(h_f, d_f, s_f)\right) \cdot (W_{cc} \cdot l_{cc}) \quad (9)$$

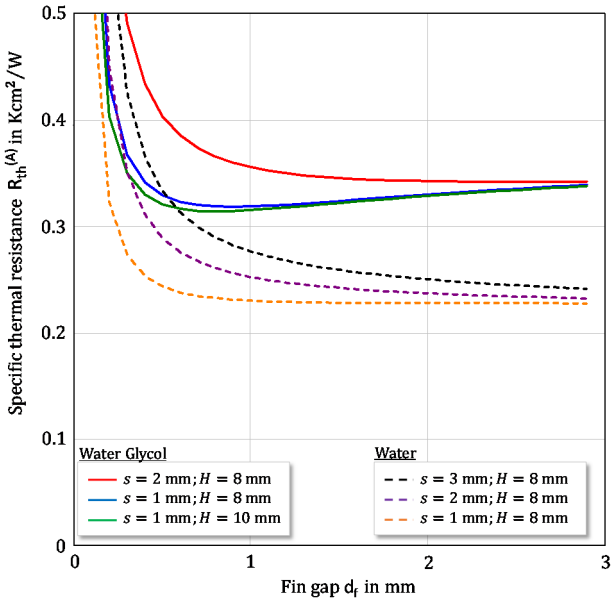

Fig. 3. Comparison of cooling options and optimum thermal resistance $R_{th}^{(A)}$.

Fig. 3 clearly shows that choosing water glycol (solid lines) is inferior as a cooling medium concerning the achievable $R_{th}^{(A)}$. Still, it is used in many inverters with a freezing point of -50 degrees Celsius. Another finding is that the fin height has less influence than the fin thickness. To emphasise this effect, only the fin thickness is used for cooling with pure water and can be easily understood from the dashed lines. Since the green and blue curves are almost similar for the selected cooling medium water glycol, a fin height of 8 mm and a fin thickness of 1 mm are optimum. In the final step, the weight of the reference heat sink (without coolant, but top plate versus bottom plate) is calculated in (10).

$$M_{hs,ref} = l_{cc} \cdot \left(W_{cc} \cdot 2 \cdot d_{ground} + s_f \cdot h_f \cdot \left[\frac{W_{cc}}{d_f + s_f}\right]\right) \cdot \rho_c \quad (10)$$

The DCB substrate Si_3N_4 is recommended and used, resulting in the following data for the inverter:

- Area-specific thermal resistance at the DCB Si_3N_4 isolator: **0.042** $\frac{\mathbf{K \cdot cm^2}}{\mathbf{W}}$
- Area-specific residual thermal resistance (chip, sintered layers, DCB metallisation): **0.02** $\frac{\boldsymbol{K \cdot cm^2}}{\boldsymbol{W}}$
- Minimum achievable area-related thermal resistance of the structured base plate (from (9)): **0.32** $\frac{\boldsymbol{K \cdot cm^2}}{\boldsymbol{W}}$
- Total area-related thermal resistance with one-sided cooling: **0.382** $\frac{\boldsymbol{K \cdot cm^2}}{\boldsymbol{W}}$
- Reference copper heat sink weight $\boldsymbol{M_{hs,ref}}$: **69.12 g**

In conclusion, the physical limits confirm the estimated cooling values in Table II.

b) Calculation of active chip area

To avoid overheating the semiconductor chip, the dissipated heat P_{th} must equal the total generated electrical loss P_{el}. For the electrical losses P_{el}, composed of switching losses P_{sw} and conduction losses P_{cond}, it is assumed that both of the respective parts are equal in an optimally designed power MOSFET [9]. Considering an additional safety margin of 25 % yields a dynamic adjustment factor for calculating the total losses of $k_{dyn} = 1.25 \cdot 2 = 2.5$. The described approach gives:

$$P_{el} = P_{cond} + P_{sw} = k_{dyn} \cdot P_{cond} = k_{dyn} \cdot I_s^2 \frac{R_{on}^{(A)}}{A_{chip}} := P_{th} = \frac{\Delta T}{R_{th}^{(A)}} A_{chip} = \frac{T_J - T_c}{R_{th}^{(A)}} A_{chip} \quad (11)$$

With the specific on-resistance $R_{on}^{(A)}$ of the transistor, the active chip area A_{chip}, the switch current Is, the junction temperature of the chip T_j and the coolant temperature Tc and the are-specific thermal resistance $R_{th}^{(A)}$. For MOSFETs, the RMS value of the switch current is related to the RMS value of the motor phase current and is calculated as a factor $k_{2L} = \frac{1}{\sqrt{2}}$. Hence, the machines modulation index and the power factor cos(φ) are completely removed from the equations [11].

$$A_{chip} = I_{AC} \cdot k_{2L} \left(\sqrt{\frac{R_{on}^{(A)} \cdot R_{th}^{(A)} \cdot k_{dyn}}{\Delta T}}\right) \quad (12)$$

In the next step, a scaling factor related to the chip area $k_{DCB} = 10$ is introduced, which allows the required DCB chip area (A_{DCB}) to be calculated from the result of (11). In addition, the base area of the heat sink A_{hs} can now be determined in (13) with the help of a constructive overhang of the heat sink relative to the DCB with $k_{hs,DCB} = 1.2$ and the weight of the associated plate-fin cooler M_{hs} in (14).

$$A_{hs} = k_{hs,DCB} \cdot A_{DCB} \quad (13)$$

$$M_{hs} = M_{hs,ref} \cdot \frac{A_{hs}}{W_{cc} \cdot L_{CC}} \quad (14)$$

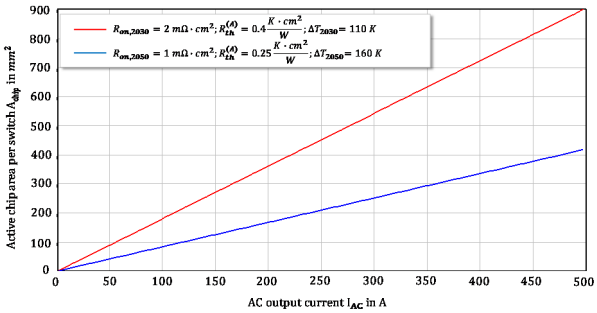

Fig. 4. Total chip area over AC output current for a 6-phase two-level inverter for 2030- and 2050-time horizons.

Finally, the calculation of the total losses and the efficiency is introduced. The calculations for the inverter's considered here are made at a DC link voltage (U_{DC}) of 800 V. This results in the total losses ($P_{losses,inv}$) in (15), the apparent power (S_{AC}) in (16) and the efficiency ($\eta_{inverter}$) of the inverter in (17). The results are presented and compared in section IV, depending on the inverters time horizon.

$$P_{losses,inv} = 6 \cdot (I_{AC} \cdot k_{2L})^2 \cdot \frac{R_{on,A} \cdot k_{dyn}}{A_{chip}} \quad (15)$$

$$S_{AC} = \sqrt{\frac{3}{2}} \cdot I_{AC,max} \cdot U_{DC} \quad (16)$$

$$\eta_{inverter} = \frac{1}{1 + \frac{P_{losses,inv}}{S_{AC}}} \quad (17)$$

c) *DC link capacitor volume estimation*

For this section, the effective value of the DC link capacitor current is estimated using (18). The capacitor RMS-current as a function of the RMS AC output current is plotted over the modulation index m_{mod} in Fig.5. The Worst-Case for the capacitor load $\boldsymbol{I_C}$ is at 0.65 I_{AC} [11].

$$I_C = I_{AC} \cdot \sqrt{\frac{m_{mod}}{(4 \cdot \pi)} \cdot \left[2\sqrt{3} \cdot (8\sqrt{3} - \frac{9\pi}{2} \cdot m_{mod}) \cos\varphi^2\right]} \quad (18)$$

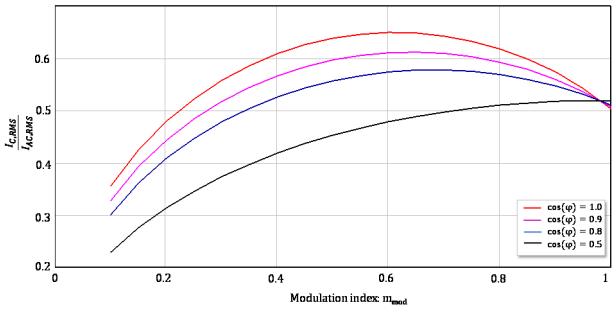

Fig. 5. Capacitor current related to modulation index for worst-case estimation

A maximum permissible voltage ripple (peak-peak; Δu_{c_pp}) of and a converter switching frequency (f_{sw}) are specified. The capacitance value needed to challenge the ripple criterion is calculated using the modulation method of [12] and (19 or 20). One considered modulation method is space vector modulation (SVPWM), and the other is discontinuous space vector modulation with a clamping angle of 60° (DPWM 60). In [12], it could be summarised that the f_{sw} is the most important reason and the DPWM 60 modulation strategy can lead to a higher voltage ripple than SVPWM. In order to consider only the absolute physical limit of the required DC link capacitance, only the first harmonic of the capacitor current $\hat{\boldsymbol{\imath}}_{\boldsymbol{c,1}}$ is considered. For DPWM, the first harmonic occurs at the switching frequency of the inverter, whereas for SVPWM the first harmonic lies at double the switching frequency [12]. For this purpose, the modulation constants from the study are introduced for the further calculation of $k_{SVPWM} = 2$ and $k_{DPWM} = 1$. Therefore, the relation at the capacitor can be expressed in terms of the impedance Z_C of the first harmonic.

$$Z_C = \frac{\hat{u}_{c_{pp}}}{\hat{\imath}_{c,1}} = \frac{\left(\frac{\Delta u_{c_{pp}}}{2}\right)}{\sqrt{2} \cdot I_C} = \frac{1}{2\pi(k_{SVPWM/DPWM} \cdot f_{sw}) C_{DC,min}} \quad (19)$$

$$C_{DC,min} = \frac{1}{2 \cdot \pi \cdot (k_{SVPWM/DPWM} \cdot f_{sw})} \cdot \frac{I_C}{\frac{\Delta u_{c\_pp}}{2 \cdot \sqrt{2}}} \quad (20)$$

From this consideration, the construction volume of the DC link capacitor can then be calculated via the required dielectric volume $V_{C,DC}$ in (21) and the weight M_C of the DC link capacitor in (22). For this purpose, the biaxially oriented polypropylene (BOPP) film is selected as the film capacitor and the material X7R as the MLLC ceramic capacitor, including its material parameters and the resulting energy density (W_{CV}).

$$V_{C,DC} = \frac{1}{2} \cdot C_{DC,min} \cdot \frac{U_{DC}^2}{W_{CV}} \quad (21)$$

$$M_C = \rho_{material} \cdot V_{C,DC} \quad (22)$$

The second criterion is calculating the required capacitor volume for the required ripple current capability. For this purpose, the power loss is first calculated as a function of the effective series resistance of the DC link capacitor $P_{losses,C,DC}$ (23) and the power loss density $P_{losses,C,DC}^{(V)}$ (24) to then determine in (25) the heating of the dielectric $\Delta T_{dielectrica}$ with (one-sided) full-surface cooling connection to the cooling plate calculated for the power module. In the next step, the required footprint area $A_{C,min}$ of the capacitor to maintain the temperature limits can be calculated with (26) and the maximum permissible thickness of the capacitor $h_{C,max}$ in the heat dissipation direction (27) [11].

$$P_{losses,C,DC} = I_C^2 \cdot R_{C,DC} \quad (23)$$

$$P_{losses,C,DC}^{(V)} = \frac{I_C^2 \cdot R_{C,DC}}{V_{C,DC}} \quad (24)$$

$$\Delta T_{dielectrica} = \frac{I_C^2 \cdot R_{C,DC} \cdot V_{C,DC}}{2 \cdot \lambda_{c,DC} \cdot A_{hs}^2} \quad (25)$$

$$A_{C,min} = \sqrt{\frac{I_C^2 \cdot R_{C,DC} \cdot V_{C,DC}}{2 \cdot \lambda_{c,DC} \cdot \Delta T_{dielectrica,max}}} \quad (26)$$

$$h_{C,max} = \frac{V_{C,DC}}{A_{C,min}} \quad (27)$$

Where $R_{C,DC}$ (0.5 mΩ) is the capacitor resistance and $\lambda_{c,DC}$ is thermal conductivity of the capacitor material according to [11].

IV. Results and Interpretation for an Aircraft Propulsion Inverter

In this section, the requirements of the drive inverter for a regional aircraft of the 50 PAX class are put into the presented model, and the results are critically evaluated. For this purpose, the specification of the drive converter with the most important basic requirements is shown in Table III.

TABLE III. Motor Specification and Resulting Requirements for SiC Inverter Configuration

Number of phases	6
Power factor cos (φ)	0.85
Number of partial inverters	2
Voltage reserve	0.1
Max. modulation index	1
The total apparent power of the inverter	652 kVA
The apparent power of partial inverters	326 kVA
Inverter AC at 800 V DC link voltage	370 A

In section III (a), it has already been shown that the assumptions for the thermal resistances for the cooling systems are close to the physical limits of the inverter and were confirmed with the mathematical model. The calculated chip areas, DCB areas, base plate weights, the losses and the efficiencies of the capacitor can be seen in Table IV. These results from the procedure are described in sections III (b) and (c). In addition, a switching frequency of 20 kHz was selected for the inverter in 2030 and a switching frequency of 40 kHz for the inverter in 2050.

For the capacitor design, only the film capacitor can be considered for the inverter 2030. The minimum area for the capacitor is 277 cm^2 and the minimum height of 5.7 mm. The size of the cooling plate is determined by the capacitor and not by the DCB area. A possible MLCC design to these criteria is unrealistic for a one-sided cooling. The calculated physical limits result in an area of 81.1 cm^2 and a minimum height of approx. 20 mm.

In conclusion, it can be mentioned that an almost 3 cm high MLCC can only be realised by stacking at least six layers of single capacitors, which cannot be thermally coupled with each other with 3.5 W/(mK). Here again, cooling on both sides would be necessary. In the case of MLCC, however, the base area of the capacitor would be comparable to the cooler area determined by the DCB area. On the other hand, considerable changes in the requirements for a DC link capacitor are considered for the year 2050, with cooling on both sides. One of the main factors for a significantly smaller capacitance is the increased switching frequency to 40 kHz, which would decrease the capacitance to $C_{DC,min,SVPWM/DPWM}$ = 85 µF/170 µF. Together with the smaller minimum capacitance, the area for a film capacitor could be reduced to 196 cm^2 and a height of 4.1 mm. However, the high current load and control should always be considered and included in the design of a DC link capacitor. Accordingly, a value of $C_{DC,min,SVPWM/DPWM}$ = 125 µF/ 250 µF is deemed realistic for a DC link capacitor. This inverter is feasible with a film capacitor, especially with cooling on both sides, which would not be problematic because of the lower total power dissipation. In addition, the total losses of the inverter are higher because of the smaller chip areas and higher operating temperatures in 2050.

TABLE IV. Results of SiC Inverters

Parameter	2030	2050
PWM switching frequency	20 kHz	40 kHz
Total losses	1.841 kW	1.986 kW
Total efficiency	99.5 %	99.5 %
Chip area per switch	112 mm^2	52 mm^2
Chip area per sub-inverter	669 mm^2	310 mm^2
DCB area per sub inverter	67 cm^2	31 cm^2
Base plate weight sub inverter	174 g	80 g
Minimum DC link capacity (SVPWM)	170 µF	125 µF
Minimum DC link capacity (DPWM)	340 µF	250 µF
Thermal conductivity of the capacitor material $\boldsymbol{\lambda_{c,DC}}$	0.3 $\frac{W}{mK}$	3.5 $\frac{W}{mK}$
Weight DC link capacitor as film capacitor (SVPWM)	0.16 kg	0.12 kg
Weight DC link capacitor as MLCC (SVPWM)	0.96 kg	0.71 kg
Volumetric power density (net volume)	128 $\frac{kVA}{L}$	200 $\frac{kVA}{L}$
Gravimetric power density (net weight)	71 $\frac{kVA}{kg}$	82 $\frac{kVA}{kg}$
Gravimetric power density (net weight)	60 $\frac{kW}{kg}$	70 $\frac{kW}{kg}$

Compared to the absolute minimum physically necessary DC link capacity stressed with one harmonic from the above academic approach in (19 or 20), a more practical design approach [13] yields the values shown in Fig.6. For 2 % of the DC link voltage or 16 V voltage ripple the minimum capacitance results with values at 204 µF/408 µF at 20 kHz and 102 µF/204 µF at 40 kHz switching frequency.

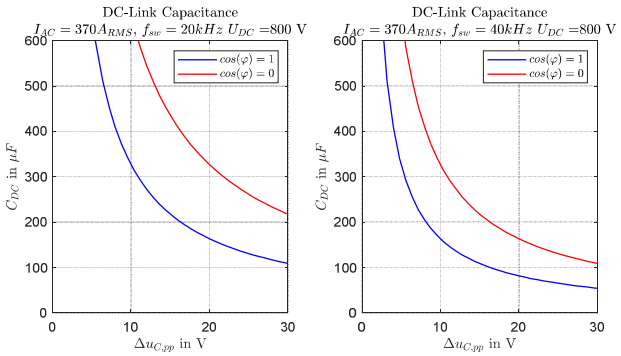

Fig. 6. Minimal DC link capacity according to the design equations described in [13]

Ultimately, it can be confirmed that the presented model can achieve the power densities of those published in the GENESIS project [14] and a state-of-the-art 600 kW Wolfspeed inverter [15]. Accordingly, the specified values for a drive inverter can be substantiated with the physical boundary conditions. With cooling on both sides and the expected smaller $R_{on}^{(A)}$, only a minimally higher power density can be achieved for potential SiC converters in the next years. Compared to a highly engineered combustion engine of a Formula 1 racing car, a physical limit of 200 kVA/L is soon reached.

According to the authors, generating 200 kVA from one litre of volume, or 200 kW from one litre of volume with a resistive load, is a physical limit and hardly conceivable. Therefore, a gravimetric power density of 82 kVA/kg is also a physical limit in today's perspective. According to the physical limitations, it might make more sense soon not to judge the research and development of a drive inverter solely based on power density, especially concerning the marginal influence of the power electronics on the overall weight of a (hybrid) electric aircraft compared to an HV battery or fuel cells. Criteria such as maximum availability, service life optimisation, and resistance to fault tolerances due to new types of separating elements would be much more interesting to address for optimising drive converters or drive trains in (hybrid) electric aviation.

V. Conclusion

This paper presents a possible design and the physical limits of a 2-level 3-phase drive inverter for future electric aircraft applications for the time horizons 2030 and 2050. The high voltage DC link voltage for both perspectives is 800 V. A method for estimating the physical limits and the resulting parameters, including the thermal management system of the power electronic converters, has been presented and discussed in this paper. In the past, power semiconductors were the enablers for higher power densities. However, the passive components and the assembly technology (incl. cooling technology) define the current physical limits. Design suggestions and details of key parameters for the inverters are given and provided for 2030 and 2050 applications. The results confirm on a physical basis the achievable power densities from recent publications and EU aerospace projects. Water glycol is proposed for cooling the converters.

In summary, 2-level inverters with conventional design will reach their physical limits if higher power density is targeted with SiC devices. Therefore, new cooling methods or operating strategies, such as cryogenic drive trains, have already arrived in the research field of propulsion concepts for aircraft. Furthermore, this study shows that the optimisation strategy for future aircraft drive inverters should determine more than the power density of an inverter.

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